General Description

The BDE-WF3235SFA module, is a 802.11abgn, IPv4 & IPv6 Low Energy module based on CC3235SF SoC.

The module offers a unique combination of lower power, integration of all external components including dual band PCB Trace Antenna at a very affordable cost.

Created for IoT , the BDE-WF3235SFA module is a wireless module that integrates two physically separated on-chip MCUs, application processor and network processor.

The BDE-WF3235SFA module is supported by easy to work with software to lower the threshold of using Wi-Fi technology or speeding up design time significantly.

The combination of affordable cost, lowest power and ease of use makes it an ideal product for the mass market, including the makers community.

## Key Features

- Fully integrated and green and RoHS modules include all required clocks, SPI flash, and passives
- 802.11a/b/g/n: 2.4 GHz and 5 GHz
- FIPS 140-2 Level 1 validated IC inside
- Multilayered security features help developers protect identities, data, and software IP
- Low-power modes for battery-powered applications
- Coexistence with 2.4-GHz radios
- Industrial temperature: –40°C to +85°C
- BDE-WF3235SFA module includes a PCB Trace Antenna for easy integration into the host system
- 1.27-mm pitch QFM package for easy assembly and low-cost PCB design
- Transferrable Wi-Fi Alliance® certification
- Application microcontroller subsystem:
  - Arm® Cortex®-M4 core at 80 MHz
  - User-dedicated memory:
    - 256KB of RAM
    - Optional 1MB of executable flash
  - Rich set of peripherals and timers:
    - McASP supports two I2S channels
    - SD, SPI, I2C, UART
    - 8-bit synchronous imager interface
    - 4-channel 12-bit ADCs
    - 4 general-purpose timers (GPT) with 16-bit PWM mode
    - Watchdog timer
    - Up to 27 GPIO pins
    - Debug interfaces: JTAG, cJTAG, SWD
- Wi-Fi network processor subsystem:
  - Wi-Fi® core:
    - 802.11 a/b/g/n 2.4 GHz and 5 GHz
    - Modes:
      - Access point (AP)
      - Station (STA)
      - Wi-Fi Direct® (only supported on 2.4GHz)
    - Security:

WEP

      - WPA™/ WPA2™ PSK
      - WPA2 Enterprise
      - WPA3™ Personal
  - Internet and application protocols:
    - HTTPs server, mDNS, DNS-SD, DHCP
    - IPv4 and IPv6 TCP/IP stack
    - 16 BSD sockets (fully secured TLS v1.2 and SSL 3.0)
  - Built-in power management subsystem:
    - Configurable low-power profiles (always on, intermittently connected, tag)
    - Advanced low-power modes
    - Integrated DC/DC regulators
- Multilayered security features:
  - Separate execution environments
  - Networking security
  - Device identity and key
  - Hardware accelerator cryptographic engines(AES, DES, SHA/MD5, CRC)
  - File system security (encryption, authentication, access control)
  - Initial secure programming
  - Software tamper detection
  - Secure boot
  - Certificate signing request (CSR)

  - Unique per device key pair
- Application throughput
  - UDP: 16 Mbps
  - TCP: 13 Mbps
- Power-Management Subsystem:
  - Integrated DC/DC converters support a wide range of supply voltage:
    - Single wide-voltage supply VBAT: 2.3 V to 3.6 V
  - Advanced low-power modes:

- Shutdown: 1 µA, Hibernate: 5.5 µA
- Low-power deep sleep (LPDS): 120 µA
- Idle connected (MCU in LPDS): 710 µA
- RX traffic (MCU active): 59 mA
- TX traffic (MCU active): 223 mA

➢ Wi-Fi TX power
- 2.4 GHz: 16 dBm at 1 DSSS
- 5 GHz: 15.1 dBm at 6 OFDM

➢ Wi-Fi RX sensitivity
- 2.4 GHz: –94.5 dBm at 1 DSSS
- 5 GHz: –89 dBm at 6 OFDM

■ Additional integrated components
➢ 40.0-MHz crystal
➢ 32.768-kHz crystal (RTC)
➢ 32Mbit SPI serial flash
➢ RF filters, diplexer and passive components

■ Footprint-compatible QFM package
➢ 1.27-mm pitch, 63-pin, 25mm × 20.5mm

■ Module supports the TI SimpleLink Developer's Ecosystem

## Applications

■ For Internet of Things applications, such as:
➢ Medical and Healthcare
- Multiparameter Patient Monitor
- Electrocardiogram (ECG)
- Electronic Hospital Bed & Bed Control
- Telehealth Systems

➢ Building and Home Automation:
- HVAC Systems & Thermostat
- Video Surveillance, Video Doorbells, and Low-Power Camera
- Building Security Systems and E-locks

➢ Appliances
➢ Asset Tracking
➢ Factory Automation
➢ Grid Infrastructure

Device Family

# Device Family

**Table 0-1. BDE-WF3235SFA Device Family**

| Part Number | Core Chip | Description | Size (mm) | Package |
|---|---|---|---|---|
| BDE-WF3235SA32 | CC3235S | With 32Mbit external flash, with PCB Trace Antenna | 20.5 × 25 × 2.4 | SMD-63 |
| BDE-WF3235SAU32 | CC3235S | With 32Mbit external flash, with U.FL connector for external antenna | 20.5 × 25 × 2.4 | SMD-63 |
| BDE-WF3235SN32 | CC3235S | With 32Mbit external flash, without antenna | 20.5 × 17.5 × 2.4 | SMD-63 |
| BDE-WF3235SFA0 | CC3235SF | Without external flash, with PCB Trace Antenna | 20.5 × 25 × 2.4 | SMD-63 |
| BDE-WF3235SFAU0 | CC3235SF | Without external flash, with U.FL connector for external antenna | 20.5 × 25 × 2.4 | SMD-63 |
| BDE-WF3235SFA32 | CC3235SF | With 32Mbit external flash, with PCB Trace Antenna | 20.5 × 25 × 2.4 | SMD-63 |
| BDE-WF3235SFAU32 | CC3235SF | With 32Mbit external flash, with U.FL connector for external antenna | 20.5 × 25 × 2.4 | SMD-63 |
| BDE-WF3235SFN0 | CC3235SF | Without external flash, without antenna | 20.5 × 17.5 × 2.4 | SMD-63 |
| BDE-WF3235SFN32 | CC3235SF | With 32Mbit external flash, without antenna | 20.5 × 17.5 × 2.4 | SMD-63 |

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# 1. References

[1] CC3235S resources: **https://www.ti.com/product/CC3235S**

[2] CC3235SF resources: **https://www.ti.com/product/CC3235SF**

## 2. Block Diagram

BDE-WF3235SFA module is based on the TI Instruments CC3235SF SoC. With an integrated 32Mbit flash, 40MHz XTAL and a dual band PCB Trace Antenna, it allows faster time to market at reduced development cost.
The module, as seen in Figure 1, comprises of:

- 32 Mbit SPI Flash
- 40MHz XTAL
- 32.768kHz XTAL
- 2 filters
- a SPDT
- a diplexer
- a dual band PCB Trace Antenna

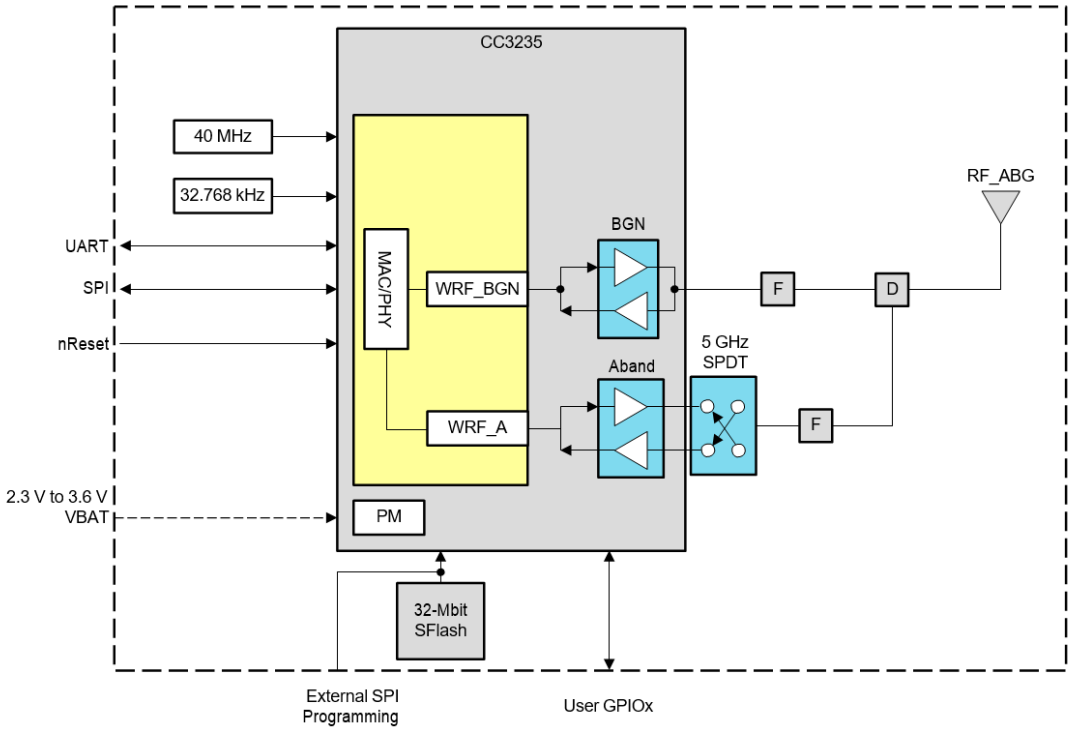


**Figure 2-1. BDE-WF3235SFA Module Block Diagram**

# 3. Terminal Configuration and Functions

## 3.1 Pin Diagram

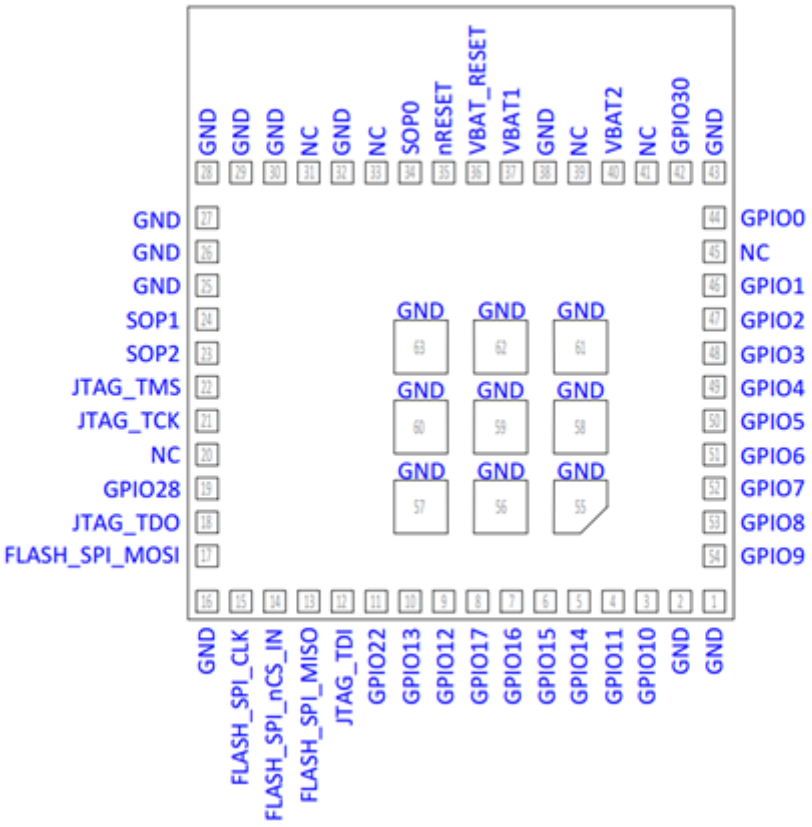


**Figure 3-1. Pin Diagram Bottom View**

## 3.2 Pin Attributes and Pin Multiplexing

**Table 3-1. Pin Description**

| Pin # | Pin Name | Type[1] | Description |
|---|---|---|---|
| 1 | GND | – | Ground |
| 2 | GND | – | Ground |
| 3 | GPIO10 | I/O | GPIO |
| 4 | GPIO11 | I/O | GPIO[2] |
| 5 | GPIO14 | I/O | GPIO[2] |
| 6 | GPIO15 | I/O | GPIO[2] |
| 7 | GPIO16 | I/O | GPIO[2] |
| 8 | GPIO17 | I/O | GPIO[2] |
| 9 | GPIO12 | I/O | GPIO[2] |
| 10 | GPIO13 | I/O | GPIO[2] |
| 11 | GPIO22 | I/O | GPIO[2] |
| 12 | JTAG_TDI | I/O | JTAG TDI input. Leave unconnected if not used on product[2] |

| Pin # | Pin Name | Type[1] | Description |
|---|---|---|---|
| 13 | FLASH_SPI_MISO | I | External serial flash programming: SPI data in |
| 14 | FLASH_SPI_nCS_IN | I | External serial flash programming: SPI chip select (active low) |
| 15 | FLASH_SPI_CLK | I | External serial flash programming: SPI clock |
| 16 | GND | – | Ground |
| 17 | FLASH_SPI_MOSI | O | External serial flash programming: SPI data out |
| 18 | JTAG_TDO | I/O | JTAG TDO output. Leave unconnected if not used on product[1] |
| 19 | GPIO28 | I/O | GPIO[2] |
| 20 | NC | – | No Connect |
| 21 | JTAG_TCK | I/O | JTAG TCK input. Leave unconnected if not used on product. [2] An internal 100-kΩ pulldown resistor is tied to this pin. |
| 22 | JTAG_TMS | I/O | JTAG TMS input. Leave unconnected if not used on product. [2] |
| 23 | SOP2 | – | An internal 100-kΩ pulldown resistor is tied to this SOP pin. An external 10-kΩ resistor is required to pull this pin high. See Section 5.11 for SOP[2:0] configuration modes. |
| 24 | SOP1 | – | An internal 100-kΩ pulldown resistor is tied to this SOP pin. An external 10-kΩ resistor is required to pull this pin high. See Section 5.11 for SOP[2:0] configuration modes. |
| 25 | GND | – | Ground |
| 26 | GND | – | Ground |
| 27 | GND | – | Ground |
| 28 | GND | – | Ground |
| 29 | GND | – | Ground |
| 30 | GND | – | Ground |
| 31 | NC | – | No Connect |
| 32 | GND | – | Ground |
| 33 | NC | – | No Connect |
| 34 | SOP0 | – | An internal 100-kΩ pulldown resistor is tied to this SOP pin. An external 10-kΩ resistor is required to pull this pin high. See Section 5.11 for SOP[2:0] configuration modes. |
| 35 | nRESET | I | There is an internal, 100-kΩ pullup resistor option from the nRESET pin to VBAT_RESET. Note: VBAT_RESET is not connected to VBAT1 or VBAT2 within the module. The following connection schemes are recommended:<br>• Connect nRESET to a switch, external controller, or host, only if nRESET will be in a defined state under all operating conditions. Leave VBAT_RESET unconnected to save power.<br>• If nRESET cannot be in a defined state under all operating conditions, connect VBAT_RESET to the main module power supply (VBAT1 and VBAT2). Due to the internal pullup resistor a leakage current of 3.3 V / 100 kΩ is expected. |
| 36 | VBAT_RESET | – | |
| 37 | VBAT1 | Power | Power supply for the module, must be connected to battery (2.3 V to 3.6 V) |
| 38 | GND | – | Ground |
| 39 | NC | – | No Connect |
| 40 | VBAT2 | Power | Power supply for the module, must be connected to battery (2.3 V to 3.6 V) |
| 41 | NC | – | No Connect |
| 42 | GPIO30 | I/O | GPIO[2] |
| 43 | GND | – | Ground |

| Pin # | Pin Name | Type(1) | Description |
|---|---|---|---|
| 44 | GPIO0 | I/O | GPIO(2) |
| 45 | NC | – | No Connect |
| 46 | GPIO1 | I/O | GPIO(2) |
| 47 | GPIO2 | I/O | GPIO(2) |
| 48 | GPIO3 | I/O | GPIO(2) |
| 49 | GPIO4 | I/O | GPIO(2) |
| 50 | GPIO5 | I/O | GPIO(2) |
| 51 | GPIO6 | I/O | GPIO(2) |
| 52 | GPIO7 | I/O | GPIO(2) |
| 53 | GPIO8 | I/O | GPIO(2) |
| 54 | GPIO9 | I/O | GPIO(2) |
| 55 | GND | – | Thermal ground |
| 56 | GND | – | Thermal ground |
| 57 | GND | – | Thermal ground |
| 58 | GND | – | Thermal ground |
| 59 | GND | – | Thermal ground |
| 60 | GND | – | Thermal ground |
| 61 | GND | – | Thermal ground |
| 62 | GND | – | Thermal ground |
| 63 | GND | – | Thermal ground |

(1) I = input; O = output; I/O = bidirectional

(2) For pin multiplexing details, see Table 3-2.

The module makes extensive use of pin multiplexing to accommodate the large number of peripheral functions in the smallest possible package. To achieve this configuration, pin multiplexing is controlled using a combination of hardware configuration (at module reset) and register control.

The board and software designers are responsible for the proper pin multiplexing configuration. Hardware does not ensure that the proper pin multiplexing options are selected for the peripherals or interface mode used. Table 3-2 describes the general pin attributes and presents an overview of pin multiplexing. All pin multiplexing options are configurable using the pin MUX registers. The following special considerations apply:

- All I/Os support drive strengths of 2, 4, and 6 mA. Drive strength is individually configurable for each pin.
- All I/Os support 10-µA pullup and pulldown resistors.
- By default, all I/Os float in the Hibernate state. However, the default state can be changed by SW.
- All digital I/Os are non fail-safe.

**Note**

If an external device drives a positive voltage to the signal pads and the BDE-WF3235SFA module is not powered, DC is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the BDE-WF3235SFA module can occur. To prevent current draw, we recommend any one of the following conditions:

- All devices interfaced to the BDE-WF3235SFA module must be powered from the same power rail as the chip.
- Use level shifters between the device and any external devices fed from other independent rails.
- The nRESET pin of the BDE-WF3235SFA module must be held low until the VBAT supply to the module is driven and stable.
- All GPIO pins default to high impedance unless programmed by the MCU. The bootloader sets the TDI, TDO, TCK, TMS, and Flash_SPI pins to mode 1. All the other pins are left in the Hi-Z state.

The ADC inputs are tolerant up to 1.8 V (see Table 4-17 for more details about the usable range of the ADC). On the other hand, the digital pads can tolerate up to 3.6 V. Hence, take care to prevent accidental damage to the ADC inputs. We recommend first disabling the output buffers of the digital I/Os corresponding to the desired ADC channel (that is, converted to Hi-Z state), and thereafter disabling the respective pass switches (S7 [Pin 47], S8 [Pin 48], S9 [Pin 49], and S10 [Pin 50]). For more information, see Table 3-4.

**Table 3-2. Pin Attributes and Pin Multiplexing**

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| kg. Pin | Pin Alias | Use | Select as Wakeup Source | Config. Addl. Analog Mux | Muxed With JTAG | Dig. Pin Mux Config. Reg. | Dig. Pin Mux Config. Mode Value | Signal Name | Signal Description | Signal Direction | LPDS | Hib | nRESET = 0 |
| 1 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 2 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 3 | GPIO10 | I/O | No | No | No | GPIO_PAD_CONFIG_10 (0x4402 E0C8) | 0 | GPIO10 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 1 | I2C_SCL | I2C clock | I/O (open drain) | Hi-Z, Pull, Drive | | |
| | | | | | | | 3 | GT_PWM06 | Pulse-width modulated O/P | O | Hi-Z, Pull, Drive | | |
| | | | | | | | 7 | UART1_TX | UART TX data | O | 1 | | |
| | | | | | | | 6 | SDCARD_CLK | SD card clock | O | 0 | | |
| | | | | | | | 12 | GT_CCP01 | Timer capture port | I | Hi-Z, Pull, Drive | | |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pkg. Pin | Pin Alias | Use | Select as Wakeup Source | Config. Addl. Analog Mux | Muxed With JTAG | Dig. Pin Mux Config. Reg. | Dig. Pin Mux Config. Mode Value | Signal Name | Signal Description | Signal Direction | LPDS | Hib | nRESET = 0 |
| 4 | GPIO11 | I/O | Yes | No | No | GPIO_PAD_CONFIG_11 (0x4402 E0CC) | 0 | GPIO11 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 1 | I2C_SDA | I2C data | I/O (open drain) | Hi-Z, Pull, Drive | | |
| | | | | | | | 3 | GT_PWM07 | Pulse-width modulated O/P | O | Hi-Z, Pull, Drive | | |
| | | | | | | | 4 | pXCLK (XVCLK) | Free clock to parallel camera | O | 0 | | |
| | | | | | | | 6 | SDCARD_CMD | SD card command line | I/O (open drain) | Hi-Z, Pull, Drive | | |
| | | | | | | | 7 | UART1_RX | UART RX data | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 12 | GT_CCP02 | Timer capture port | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 13 | MCAFSX | I2S audio port frame sync | O | Hi-Z, Pull, Drive | | |
| 5 | GPIO14 | I/O | No | No | No | GPIO_PAD_CONFIG_14 (0x4402 E0D8) | 0 | GPIO14 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 5 | I2C_SCL | I2C clock | I/O (open drain) | | | |
| | | | | | | | 7 | GSPI_CLK | General SPI clock | I/O | | | |
| | | | | | | | 4 | pDATA8(CAM_D4) | Parallel camera data bit 4 | I | | | |
| | | | | | | | 12 | GT_CCP05 | Timer capture port | I | | | |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pkg. Pin | Pin Alias | Use | Select as Wakeup Source | Config. Addl. Analog Mux | Muxed With JTAG | Dig. Pin Mux Config. Reg. | Dig. Pin Mux Config. Mode Value | Signal Name | Signal Description | Signal Direction | LPDS | Hib | nRESET = 0 |
| 6 | GPIO15 | I/O | No | No | No | GPIO_PAD_CONFIG_15 (0x4402 E0DC) | 0 | GPIO15 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 5 | I2C_SDA | I2C data | I/O (open drain) | | | |
| | | | | | | | 7 | GSPI_MISO | General SPI MISO | I/O | | | |
| | | | | | | | 4 | pDATA9 (CAM_D5) | Parallel camera data bit 5 | I | | | |
| | | | | | | | 13 | GT_CCP06 | Timer capture port | I | | | |
| | | | | | | | 8 | SDCARD_DATA0 | SD card data | I/O | | | |
| 7 | GPIO16 | I/O | No | No | No | GPIO_PAD_CONFIG_16 (0x4402 E0E0) | 0 | GPIO16 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | | | | | Hi-Z, Pull, Drive | | |
| | | | | | | | | | | | Hi-Z, Pull, Drive | | |
| | | | | | | | 7 | GSPI_MOSI | General SPI MOSI | I/O | Hi-Z, Pull, Drive | | |
| | | | | | | | 4 | pDATA10 (CAM_D6) | Parallel camera data bit 6 | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 5 | UART1_TX | UART1 TX data | O | 1 | | |
| | | | | | | | 13 | GT_CCP07 | Timer capture port | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 8 | SDCARD_CLK | SD card clock | O | Zero | | |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pkg. Pin | Pin Alias | Use | Select as Wakeup Source | Config. Addl. Analog Mux | Muxed With JTAG | Dig. Pin Mux Config. Reg. | Dig. Pin Mux Config. Mode Value | Signal Name | Signal Description | Signal Direction | LPDS | Hib | nRESET = 0 |
| 8 | GPIO17 | I/O | Yes | No | No | GPIO_PAD_CONFIG_17 (0x4402 E0E4) | 0 | GPIO17 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 5 | UART1_RX | UART1 RX data | I | | | |
| | | | | | | | 7 | GSPI_CS | General SPI chip select | I/O | | | |
| | | | | | | | 4 | pDATA11 (CAM_D7) | Parallel camera data bit 7 | I | | | |
| | | | | | | | 8 | SDCARD_CMD | SD card command line | I/O | | | |
| 9 | GPIO12 | I/O | No | No | No | GPIO_PAD_CONFIG_12 (0x4402 E0D0) | 0 | GPIO12 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 3 | McACLK | $I^2S$ audio port clock output | O | Hi-Z, Pull, Drive | | |
| | | | | | | | 4 | pVS (VSYNC) | Parallel camera vertical sync | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 5 | I2C_SCL | $I^2C$ clock | I/O (open drain) | Hi-Z, Pull, Drive | | |
| | | | | | | | 7 | UART0_TX | UART0 TX data | O | 1 | | |
| | | | | | | | 12 | GT_CCP03 | Timer capture port | I | Hi-Z, Pull, Drive | | |
| 10 | GPIO13 | I/O | Yes | No | No | GPIO_PAD_CONFIG_13 (0x4402 E0D4) | 0 | GPIO13 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 5 | I2C_SDA | $I_2C$ data | I/O (open drain) | | | |
| | | | | | | | 4 | pHS (HSYNC) | Parallel camera horizontal sync | I | | | |
| | | | | | | | 7 | UART0_RX | UART0 RX data | I | | | |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | 12 | GT_CCP04 | Timer capture port | I | | | |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pkg. Pin | Pin Alias | Use | Select as Wakeup Source | Config. Addl. Analog Mux | Muxed With JTAG | Dig. Pin Mux Config. Reg. | Dig. Pin Mux Config. Mode Value | Signal Name | Signal Description | Signal Direction | LPDS | Hib | nRESET = 0 |
| 11 | GPIO22 | I/O | No | No | No | GPIO_PAD_CONFIG_22 (0x4402 E0F8) | 0 | GPIO22 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 7 | McAFSX | I2S audio port frame sync | O | | | |
| | | | | | | | 5 | GT_CCP04 | Timer capture port | I | | | |
| 12 | JTAG_TDI | I/O | No | No | Muxed with JTAG TDI | GPIO_PAD_CONFIG_23 (0x4402 E0FC) | 1 | TDI | JTAG TDI. Reset default pinout. | I | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 0 | GPIO23 | GPIO | I/O | | | |
| | | | | | | | 2 | UART1_TX | UART1 TX data | O | 1 | | |
| | | | | | | | 9 | I2C_SCL | I2C clock | I/O (open drain) | Hi-Z, Pull, Drive | | |
| 13 | FLASH_ SPI_ MISO | N/A | N/A | N/A | N/A | N/A | N/A | FLASH_SPI_MISO | Data from SPI serial flash (fixed default) | N/A | Hi-Z | Hi-Z | Hi-Z |
| 14 | FLASH_ SPI_nCS_IN | N/A | N/A | N/A | N/A | N/A | N/A | FLASH_SPI_nCS_ IN | Chip select to SPI serial flash (fixed default) | N/A | 1 | Hi-Z, Pull, Drive | Hi-Z |
| 15 | FLASH_ SPI_CLK | N/A | N/A | N/A | N/A | N/A | N/A | FLASH_SPI_ CLK | Clock to SPI serial flash (fixed default) | N/A | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| 16 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 17 | FLASH_ SPI_ MOSI | N/A | N/A | N/A | N/A | N/A | N/A | FLASH_SPI_MOSI | Data to SPI serial flash (fixed default) | N/A | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pkg. Pin | Pin Alias | Use | Select as Wakeup Source | Config. Addl. Analog Mux | Muxed With JTAG | Dig. Pin Mux Config. Reg. | Dig. Pin Mux Config. Mode Value | Signal Name | Signal Description | Signal Direction | LPDS | Hib | nRESET = 0 |
| 18 | JTAG_TDO | I/O | Yes | No | Muxed with JTAG TDO | GPIO_PAD_ CONFIG_ 24 (0x4402 E100) | 1 | TDO | JTAG TDO. Reset default pinout. | O | Hi-Z, Pull, Drive | Driven high in SWD; driven low in 4- wire JTAG | Hi-Z |
| | | | | | | | 0 | GPIO24 | GPIO | I/O | | | |
| | | | | | | | 5 | PWM0 | Pulse-width modulated O/P | O | | | |
| | | | | | | | 2 | UART1_RX | UART1 RX data | I | | | |
| | | | | | | | 9 | I2C_SDA | I2C data | I/O (open drain) | | | |
| | | | | | | | 4 | GT_CCP06 | Timer capture port | I | | | |
| | | | | | | | 6 | McAFSX | I2S audio port frame sync | O | | | |
| 19 | GPIO28 | I/O | No | No | No | GPIO_PAD_ CONFIG_ 40 (0x4402 E140) | 0 | GPIO28 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| 20 | NC | WLAN analog | N/A | N/A | N/A | N/A | N/A | NC | Reserved | N/A | N/A | N/A | N/A |
| 21 | JTAG_TCK | I/O | No | No | Muxed with JTAG/ SWD- TCK | GPIO_PAD_ CONFIG_ 28 (0x4402 E110) | 1 | TCK | JTAG/SWD TCK. Reset default pinout. | I | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 8 | GT_PWM03 | Pulse-width modulated O/P | O | | | |
| 22 | JTAG_TMS | I/O | No | No | Muxed with JTAG/ SWD- TMSC | GPIO_PAD_ CONFIG_ 29 (0x4402 E114) | 1 | TMS | JTAG/SWD TMS. Reset default pinout. | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 0 | GPIO29 | GPIO | | | | |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pkg. Pin | Pin Alias | Use | Select as Wakeup Source | Config. Addl. Analog Mux | Muxed With JTAG | Dig. Pin Mux Config. Reg. | Dig. Pin Mux Config. Mode Value | Signal Name | Signal Description | Signal Direction | LPDS | Hib | nRESET = 0 |
| 23 | SOP2 | O only | No | No | No | GPIO_PAD_CONFIG_ 25 (0x4402 E104) | 0 | GPIO25 | GPIO | O | Hi-Z, Pull, Drive | Driven Low | Hi-Z |
| | | | | | | | 9 | GT_PWM02 | Pulse-width modulated O/P | O | Hi-Z, Pull, Drive | | |
| | | | | | | | 2 | McAFSX | I2S audio port frame sync | O | Hi-Z, Pull, Drive | | |
| | | | | | | | | TCXO_EN | Enable to optional external 40-MHz TCXO | O | 0 | | |
| | | | | | | | | SOP2 | Sense-on-power 2 | I | Hi-Z, Pull, Drive | | |
| 24 | SOP1 | Config sense | N/A | N/A | N/A | N/A | N/A | SOP1 | Sense-on-power 1 | N/A | N/A | N/A | N/A |
| 25 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 26 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 27 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 28 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 29 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 30 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 31 | NC | WLAN analog | N/A | N/A | N/A | N/A | | NC | Reserved | | | | |
| 32 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 33 | NC | WLAN analog | N/A | N/A | N/A | N/A | | NC | Reserved | | | | |
| 34 | SOP0 | Config sense | N/A | N/A | N/A | N/A | N/A | SOP0 | Sense-on-power 0 | N/A | N/A | N/A | N/A |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 35 | nRESET | Global reset | N/A | N/A | N/A | N/A | N/A | nRESET | Master chip reset. Active low. | N/A | N/A | N/A | N/A |
| 36 | VBAT_ RESET | Global reset | N/A | N/A | N/A | N/A | N/A | VBAT_RESET | VBAT to nRESET pullup resistor | N/A | N/A | N/A | N/A |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pkg. Pin** | **Pin Alias** | **Use** | **Select as Wakeup Source** | **Config. Addl. Analog Mux** | **Muxed With JTAG** | **Dig. Pin Mux Config. Reg.** | **Dig. Pin Mux Config. Mode Value** | **Signal Name** | **Signal Description** | **Signal Direction** | **LPDS** | **Hib** | **nRESET = 0** |
| 37 | VBAT1 | Supply input | N/A | N/A | N/A | N/A | N/A | VBAT1 | Analog DC/DC input (connected to chip input supply [VBAT]) | N/A | N/A | N/A | N/A |
| 38 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 39 | NC | WLAN analog | N/A | N/A | N/A | N/A | N/A | NC | Reserved | N/A | N/A | N/A | N/A |
| 40 | VBAT2 | Supply input | N/A | N/A | N/A | N/A | N/A | VBAT2 | Analog input supply VBAT | N/A | N/A | N/A | N/A |
| 41 | NC | WLAN analog | N/A | N/A | N/A | N/A | N/A | NC | Reserved | N/A | N/A | N/A | N/A |
| 42 | GPIO30 | I/O | No | User config not required | No | GPIO_PAD_ CONFIG_30 (0x4402 E118) | 0 | GPIO30 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 9 | UART0_TX | UART0 TX data | O | 1 | | |
| | | | | | | | 2 | McACLK | I2S audio port clock | O | Hi-Z, Pull, Drive | | |
| | | | | | | | 3 | McAFSX | I2S audio port frame sync | O | Hi-Z, Pull, Drive | | |
| | | | | | | | 4 | GT_CCP05 | Timer capture port | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 7 | GSPI_MISO | General SPI MISO | I/O | Hi-Z, Pull, Drive | | |
| 43 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pkg. Pin | Pin Alias | Use | Select as Wakeup Source | Config. Addl. Analog Mux | Muxed With JTAG | Dig. Pin Mux Config. Reg. | Dig. Pin Mux Config. Mode Value | Signal Name | Signal Description | Signal Direction | LPDS | Hib | nRESET = 0 |
| 44 | GPIO0 | I/O | No | User config not required | No | GPIO_PAD_ CONFIG_0 (0x4402 E0A0) | 0 | GPIO0 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 12 | UART0_CTS | UART0 Clear-to- Send input (active low) | I | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 6 | McAXR1 | I2S audio port data 1 (RX/TX) | I/O | Hi-Z, Pull, Drive | | |
| | | | | | | | 7 | GT_CCP00 | Timer capture port | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 9 | GSPI_CS | General SPI chip select | I/O | Hi-Z, Pull, Drive | | |
| | | | | | | | 10 | UART1_RTS | UART1 Request-to-Send (active low) | O | 1 | | |
| | | | | | | | 3 | UART0_RTS | UART0 Request-to-Send (active low) | O | 1 | | |
| | | | | | | | 4 | McAXR0 | I2S audio port data 0 (RX/TX) | I/O | Hi-Z, Pull, Drive | | |
| 45 | NC | WLAN | N/A | N/A | N/A | N/A | N/A | NC | Reserved | N/A | N/A | N/A | N/A |
| 46 | GPIO1 | I/O | No | No | No | GPIO_PAD_ CONFIG_1 (0x4402 E0A4) | 0 | GPIO1 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 3 | UART0_TX | UART0 TX data | O | 1 | | |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | 4 | pCLK (PIXCLK) | Pixel clock from parallel camera sensor | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 6 | UART1_TX | UART1 TX data | O | 1 | | |
| | | | | | | | 7 | GT_CCP01 | Timer capture port | I | Hi-Z, Pull, Drive | | |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pkg. Pin** | **Pin Alias** | **Use** | **Select as Wakeup Source** | **Config. Addl. Analog Mux** | **Muxed With JTAG** | **Dig. Pin Mux Config. Reg.** | **Dig. Pin Mux Config. Mode Value** | **Signal Name** | **Signal Description** | **Signal Direction** | **LPDS** | **Hib** | **nRESET = 0** |
| 47 | GPIO2 | Analog input (up to 1.8 V)/ digital I/O | Yes | | No | GPIO_PAD_CONFIG_2 (0x4402 E0A8) | | ADC_CH0 | ADC channel 0 input (1.5-V max) | I | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 0 | GPIO2 | GPIO | I/O | Hi-Z, Pull, Drive | | |
| | | | | | | | 3 | UART0_RX | UART0 RX data | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 6 | UART1_RX | UART1 RX data | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 7 | GT_CCP02 | Timer capture port | I | Hi-Z, Pull, Drive | | |
| 48 | GPIO3 | Analog input (up to 1.8 V)/ digital I/O | No | | No | GPIO_PAD_CONFIG_3 (0x4402 E0AC) | | ADC_CH1 | ADC channel 1 input (1.5-V max) | I | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 0 | GPIO3 | GPIO | I/O | Hi-Z, Pull, Drive | | |
| | | | | | | | 6 | UART1_TX | UART1 TX data | O | 1 | | |
| | | | | | | | 4 | pDATA7 (CAM_D3) | Parallel camera data bit 3 | I | Hi-Z, Pull, Drive | | |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pkg. Pin** | **Pin Alias** | **Use** | **Select as Wakeup Source** | **Config. Addl. Analog Mux** | **Muxed With JTAG** | **Dig. Pin Mux Config. Reg.** | **Dig. Pin Mux Config. Mode Value** | **Signal Name** | **Signal Description** | **Signal Direction** | **LPDS** | **Hib** | **nRESET = 0** |
| 49 | GPIO4 | Analog input (up to 1.8 V)/ digital I/O | Yes | | Yes | GPIO_PAD_ CONFIG_4 (0x4402 E0B0) | | ADC_CH2 | ADC channel 2 input (1.5-V max) | I | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 0 | GPIO4 | GPIO | I/O | Hi-Z, Pull, Drive | | |
| | | | | | | | 6 | UART1_RX | UART1 RX data | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 4 | pDATA6 (CAM_D2) | Parallel camera data bit 2 | I | Hi-Z, Pull, Drive | | |
| 50 | GPIO5 | Analog input up to 1.5 V | No | | No | GPIO_PAD_ CONFIG_5 (0x4402 E0B4) | | ADC_CH3 | ADC channel 3 input (1.5 V max) | I | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 0 | GPIO5 | GPIO | I/O | Hi-Z, Pull, Drive | | |
| | | | | | | | 4 | pDATA5 (CAM_D1) | Parallel camera data bit 1 | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 6 | McAXR1 | I2S audio port data 1 (RX, TX) | I/O | Hi-Z, Pull, Drive | | |
| | | | | | | | 7 | GT_CCP05 | Timer capture port | I | Hi-Z, Pull, Drive | | |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pkg. Pin | Pin Alias | Use | Select as Wakeup Source | Config. Addl. Analog Mux | Muxed With JTAG | Dig. Pin Mux Config. Reg. | Dig. Pin Mux Config. Mode Value | Signal Name | Signal Description | Signal Direction | LPDS | Hib | nRESET = 0 |
| 51 | GPIO6 | I/O | No | No | No | GPIO_PAD_CONFIG_6 (0x4402 E0B8) | 0 | GPIO6 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 5 | UART0_RTS | UART0 Request-to-Send (active low) | O | 1 | | |
| | | | | | | | 4 | pDATA4 (CAM_D0) | Parallel camera data bit 0 | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 3 | UART1_CTS | UART1 Clear to send (active low) | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 6 | UART0_CTS | UART0 Clear to send (active low) | I | Hi-Z, Pull, Drive | | |
| | | | | | | | 7 | GT_CCP06 | Timer capture port | I | Hi-Z, Pull, Drive | | |
| 52 | GPIO7 | I/O | No | No | No | GPIO_PAD_CONFIG_7 (0x4402 E0BC) | 0 | GPIO7 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 13 | McACLK | I2S audio port clock | O | Hi-Z, Pull, Drive | | |
| | | | | | | | 3 | UART1_RTS | UART1 Request to send (active low) | O | 1 | | |
| | | | | | | | 10 | UART0_RTS | UART0 Request to send (active low) | O | 1 | | |
| | | | | | | | 11 | UART0_TX | UART0 TX data | O | 1 | | |
| 53 | GPIO8 | I/O | No | No | No | GPIO_PAD_CONFIG_8 | 0 | GPIO8 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, | Hi-Z |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | (0x4402 E0C0) | 6 | SDCARD_IRQ | Interrupt from SD card (future support) | I | | Drive | |
| | | | | | | | 7 | McAFSX | I2S audio port frame sync | O | | | |
| | | | | | | | 12 | GT_CCP06 | Timer capture port | I | | | |

| GENERAL PIN ATTRIBUTES | | | | | | FUNCTION | | | | | PAD STATES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pkg. Pin** | **Pin Alias** | **Use** | **Select as Wakeup Source** | **Config. Addl. Analog Mux** | **Muxed With JTAG** | **Dig. Pin Mux Config. Reg.** | **Dig. Pin Mux Config. Mode Value** | **Signal Name** | **Signal Description** | **Signal Direction** | **LPDS** | **Hib** | **nRESET = 0** |
| 54 | GPIO9 | I/O | No | No | No | GPIO_PAD_ CONFIG_9 (0x4402 E0C4) | 0 | GPIO9 | GPIO | I/O | Hi-Z, Pull, Drive | Hi-Z, Pull, Drive | Hi-Z |
| | | | | | | | 3 | GT_PWM05 | Pulse-width modulated O/P | O | | | |
| | | | | | | | 6 | SDCARD_ DATA0 | SD card data | I/O | | | |
| | | | | | | | 7 | McAXR0 | I2S audio port data (RX, TX) | I/O | | | |
| | | | | | | | 12 | GT_CCP00 | Timer capture port | I | | | |
| 55 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 56 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 57 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 58 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 59 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 60 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 61 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |
| 62 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 63 | GND | GND | N/A | N/A | N/A | N/A | N/A | GND | GND | N/A | N/A | N/A | N/A |

## 3.3 Signal Descriptions

**Table 3-3. Signal Descriptions**

| FUNCTION | SIGNAL NAME | PIN NO. | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION |
|---|---|---|---|---|---|
| ADC | ADC_CH0 | 47 | I/O | I | ADC channel 0 input (maximum of 1.5 V) |
| | ADC_CH1 | 48 | I/O | I | ADC channel 1 input (maximum of 1.5 V) |
| | ADC_CH2 | 49 | I/O | I | ADC channel 2 input (maximum of 1.5 V) |
| | ADC_CH3 | 50 | I | I | ADC channel 3 input (maximum of 1.5 V) |
| BLE/2.4 GHz radio coexistence (2) | GPIO10 | 3 | I/O | I/O | Coexistence inputs and outputs |
| | GPIO14 | 5 | I/O | I/O | |
| | GPIO15 | 6 | I/O | I/O | |
| | GPIO16 | 7 | I/O | I/O | |
| | GPIO17 | 8 | I/O | I/O | |
| | GPIO12 | 9 | I/O | I/O | |
| | GPIO22 | 11 | I/O | I/O | |
| | GPIO28 | 19(1) | I/O | I/O | |
| | GPIO0 | 44 | I/O | I/O | |
| | GPIO30 | 42(1) | I/O | I/O | |
| | GPIO5 | 50 | I/O | I/O | |
| | GPIO6 | 51 | I/O | I/O | |
| | GPIO8 | 53 | I/O | I/O | |
| | GPIO9 | 54 | I/O | I/O | |
| Hostless mode | HM_IO | 3 | I/O | I/O | Hostless mode inputs and outputs |
| | | 4 | I/O | O | |
| | | 5 | I/O | I/O | |
| | | 6 | I/O | I/O | |
| | | 7 | I/O | I/O | |
| | | 8 | I/O | I/O | |
| | | 9 | I/O | I/O | |
| | | 10 | I/O | O | |
| | | 11 | I/O | I/O | |
| | | 19(1) | I/O | I/O | |
| | | 23 | O | O | |
| | | 42(1) | I/O | I/O | |
| | | 44 | I/O | I/O | |
| | | 48 | O | O | |
| | | 49 | O | O | |
| | | 50 | I/O | I/O | |
| | | 51 | I/O | I/O | |
| | | 53 | I/O | I/O | |
| | | 54 | I/O | I/O | |
| JTAG / SWD | TDI | 12 | I/O | I | JTAG TDI. Reset default pinout. |
| | TDO | 18 | I/O | O | JTAG TDO. Reset default pinout. |
| | TCK | 21 | I/O | I | JTAG/SWD TCK. Reset default pinout. |
| | TMS | 22 | I/O | I/O | JTAG/SWD TMS. Reset default pinout. |

| FUNCTION | SIGNAL NAME | PIN NO. | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION |
|---|---|---|---|---|---|
| $I^2C$ | I2C_SCL | 3 | I/O | I/O (open drain) | $I^2C$ clock data |
| | | 5 | | | |
| | | 9 | | | |
| | | 12 | | | |
| | I2C_SDA | 4 | I/O | I/O (open drain) | $I^2C$ data |
| | | 6 | | | |
| | | 10 | | | |
| | | 18 | | | |
| Timers | GT_PWM06 | 3 | I/O | O | Pulse-width modulated O/P |
| | GT_CCP01 | 46 | I/O | I | Timer capture port |
| | GT_PWM07 | 4 | I/O | O | Pulse-width modulated O/P |
| | GT_CCP02 | 47 | I/O | I | Timer capture ports |
| | GT_CCP03 | 9 | I/O | I | |
| | GT_CCP04 | 10 | I/O | I | |
| | | 11 | I/O | I | |
| | GT_CCP05 | 5 | I/O | I | |
| | GT_CCP06 | 6 | I/O | I | |
| | | 18 | I/O | I | |
| | | 51 | I/O | I | |
| | | 53 | I/O | I | |
| | GT_CCP07 | 7 | I/O | I | |
| | PWM0 | 18 | I/O | O | Pulse-width modulated outputs |
| | GT_PWM03 | 21 | I/O | O | |
| | GT_PWM02 | 23 | O | O | |
| | GT_CCP00 | 44 | I/O | I | Timer capture ports |
| | | 54 | I/O | I | |
| | GT_CCP05 | 42 | I/O | I | |
| | GT_CCP01 | 46 | I/O | I | |
| | GT_CCP02 | 47 | I/O | I | |
| | GT_CCP05 | 50 | I | I | Timer capture port Input |
| | GT_PWM05 | 54 | I/O | O | Pulse-width modulated output |

| FUNCTION | SIGNAL NAME | PIN NO. | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION |
|---|---|---|---|---|---|
| GPIO | GPIO10 | 3 | I/O | I/O | General-purpose inputs or outputs |
| | GPIO11 | 4 | I/O | I/O | |
| | GPIO14 | 5 | I/O | I/O | |
| | GPIO15 | 6 | I/O | I/O | |
| | GPIO16 | 7 | I/O | I/O | |
| | GPIO17 | 8 | I/O | I/O | |
| | GPIO12 | 9 | I/O | I/O | |
| | GPIO13 | 10 | I/O | I/O | |
| | GPIO22 | 11 | I/O | I/O | |
| | GPIO23 | 12 | I/O | I/O | |
| | GPIO24 | 18 | I/O | I/O | |
| | GPIO28 | 19 | I/O | I/O | |
| | GPIO29 | 22 | I/O | I/O | |
| | GPIO25 | 23 | O | O | |
| | GPIO0 | 44 | I/O | I/O | |
| | GPIO30 | 42 | I/O | I/O | |
| | GPIO1 | 46 | I/O | I/O | |
| | GPIO2 | 47 | I/O | I/O | |
| | GPIO3 | 48 | I/O | I/O | |
| | GPIO4 | 49 | I/O | I/O | |
| | GPIO5 | 50 | I/O | I/O | |
| | GPIO6 | 51 | I/O | I/O | |
| | GPIO7 | 52 | I/O | I/O | |
| | GPIO8 | 53 | I/O | I/O | |
| | GPIO9 | 54 | I/O | I/O | |
| McASP<br>I²S or PCM | MCAFSX | 4 | I/O | O | I²S audio port frame sync |
| | | 11 | | | |
| | | 18 | | | |
| | | 23 | | | |
| | | 42 | | | |
| | | 53 | | | |
| | McACLK | 9 | I/O | O | I²S audio port clock outputs |
| | | 42 | I/O | O | |
| | McAXR1 | 44 | I/O | I/O | I²S audio port data 1 (RX/TX) |
| | | 50 | I | I/O | I²S audio port data 1 (RX and TX) |
| | McAXR0 | 44 | I/O | I/O | I²S audio port data 0 (RX and TX) |
| | | 54 | I/O | I/O | I²S audio port data (RX and TX) |
| | McACLKX | 52 | I/O | O | I²S audio port clock |
| Multimedia card (MMC or SD) | SDCARD_CLK | 3 | I/O | O | SD card clock data |
| | | 7 | | | |
| | SDCARD_CMD | 4 | I/O | I/O (open drain) | SD card command line |
| | | 8 | I/O | I/O | |
| | SDCARD_DATA0 | 6 | I/O | I/O | SD card data |
| | | 54 | | | |
| | SDCARD_IRQ | 53 | I/O | I | Interrupt from SD card(3) |

| FUNCTION | SIGNAL NAME | PIN NO. | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION |
|---|---|---|---|---|---|
| Parallel interface (8-bit π) | pXCLK (XVCLK) | 4 | I/O | O | Free clock to parallel camera |
| | pVS (VSYNC) | 9 | I/O | I | Parallel camera vertical sync |
| | pHS (HSYNC) | 10 | I/O | I | Parallel camera horizontal sync |
| | pDATA8 (CAM_D4) | 5 | I/O | I | Parallel camera data bit 4 |
| | pDATA9 (CAM_D5) | 6 | I/O | I | Parallel camera data bit 5 |
| | pDATA10 (CAM_D6) | 7 | I/O | I | Parallel camera data bit 6 |
| | pDATA11 (CAM_D7) | 8 | I/O | I | Parallel camera data bit 7 |
| | pCLK (PIXCLK) | 46 | I/O | I | Pixel clock from parallel camera sensor |
| | pDATA7 (CAM_D3) | 48 | I/O | I | Parallel camera data bit 3 |
| | pDATA6 (CAM_D2) | 49 | I/O | I | Parallel camera data bit 2 |
| | pDATA5 (CAM_D1) | 50 | I | I | Parallel camera data bit 1 |
| | pDATA4 (CAM_D0) | 51 | I/O | I | Parallel camera data bit 0 |
| Power | VBAT1 | 37 | — | — | Power supply for the module |
| | VBAT2 | 40 | — | — | Power supply for the module |
| SPI | GSPI_CLK | 5 | I/O | I/O | General SPI clock |
| | GSPI_MISO | 6 | I/O | I/O | General SPI MISO |
| | | 42 | I/O | I/O | |
| | GSPI_CS | 8 | I/O | I/O | General SPI device select |
| | | 44 | I/O | I/O | |
| | GSPI_MOSI | 7 | I/O | I/O | General SPI MOSI |
| FLASH SPI | FLASH_SPI_CLK | 15 | O | O | Clock to SPI serial flash (fixed default) |
| | FLASH_SPI_DOUT | 17 | O | O | Data to SPI serial flash (fixed default) |
| | FLASH_SPI_DIN | 13 | I | I | Data from SPI serial flash (fixed default) |
| | FLASH_SPI_CS | 14 | O | O | Device select to SPI serial flash (fixed default) |

| FUNCTION | SIGNAL NAME | PIN NO. | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION |
|---|---|---|---|---|---|
| UART | UART1_TX | 3 | I/O | O | UART TX data |
| | | 7 | I/O | O | |
| | | 12 | I/O | O | |
| | | 46 | I/O | O | |
| | | 48 | I/O | O | UART1 TX data |
| | UART1_RX | 4 | I/O | I | UART RX data |
| | | 8 | I/O | I | |
| | | 18 | I/O | I | |
| | | 47 | I/O | I | UART1 RX data |
| | | 49 | I/O | I | |
| | UART1_RTS | 44 | I/O | O | UART1 request-to-send (active low) |
| | | 52 | I/O | O | |
| | UART1_CTS | 51 | I/O | I | UART1 clear-to-send (active low) |
| | UART0_TX | 9 | I/O | O | UART0 TX data |
| | | 42 | I/O | O | |
| | | 46 | I/O | O | |
| | | 52 | I/O | O | |
| | UART0_RX | 10 | I/O | I | UART0 RX data |
| | | 47 | I/O | I | UART0 RX data |
| | UART0_CTS | 44 | I/O | I | UART0 clear-to-send input (active low) |
| | | 51 | | | |
| | UART0_RTS | 44 | I/O | O | UART0 request-to-send (active low) |
| | | 51 | I/O | O | |
| | | 52 | I/O | O | |
| Sense-On-Power | SOP2 | 23(4) | O | I | Sense-on-power 2 |
| | SOP1 | 24 | I | I | Configuration sense-on-power 1 |
| | SOP0 | 34 | I | I | Configuration sense-on-power 0 |

(1) LPDS retention unavailable.

(2) The BDE-WF3235SFA module is compatible with TI BLE modules using an external RF switch.

(3) Future support.

(4) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.

## 3.4 Drive Strength and Reset States for Analog-Digital Multiplexed Pins

Table 3-4 describes the use, drive strength, and default state of analog- and digital-multiplexed pins at first-time power up and reset (nRESET pulled low).

**Table 3-4. Drive Strength and Reset States for Analog-Digital Multiplexed Pins**

| PIN | BOARD LEVEL CONFIGURATION AND USE | DEFAULT STATE AT FIRST POWER UP OR FORCED RESET | STATE AFTER CONFIGURATION OF ANALOG SWITCHES (ACTIVE, LPDS, and HIB POWER MODES) | MAXIMUM EFFECTIVE DRIVE STRENGTH (mA) |
|---|---|---|---|---|
| 42 | Generic I/O | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 44 | Generic I/O | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 47 | Analog signal (1.8-V absolute, 1.46-V full scale) | ADC is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 48 | Analog signal (1.8-V absolute, 1.46-V full scale) | ADC is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 49 | Analog signal (1.8-V absolute, 1.46-V full scale) | ADC is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 50 | Analog signal (1.8-V absolute, 1.46-V full scale) | ADC is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |

## 3.5 Pad State After Application of Power to Chip, but Before Reset Release

When a stable power is applied to the BDE-WF3235SFA module for the first time or when supply voltage is restored to the proper value following a prior period with supply voltage below 1.5V, the level of the digital pads are undefined in the period starting from the release of nRESET and until the DIG_DCDC of the CC3235SF chip powers up. This period is less than approximately 10ms. During this period, pads can be internally pulled weakly in either direction. If a certain set of pins are required to have a definite value during this pre-reset period, an appropriate pullup or pulldown must be used at the board level. The recommended value of these external pullup or pulldown resistors is 2.7kΩ.

## 3.6 Connections for Unused Pins

All unused pin should be configured as stated in Table 3-5.

**Table 3-5. Connections for Unused Pins**

| FUNCTION | SIGNAL DESCRIPTION | PIN NUMBER | ACCEPTABLE PRACTICE |
|---|---|---|---|
| GPIO | General-purpose input or output | | Wake up I/O source should not be floating during hibernate. All the I/O pins will float while in Hibernate and Reset states. Ensure pullup and pulldown resistors are available on board to maintain the state of the I/O. Leave unused GPIOs as NC |
| No Connect | NC | 20, 31, 33, 39, 41, 45 | Unused pin, leave as NC. |
| SOP | Configuration sense-on-power | 23, 24, 34 | Leave as NC (Modules contain internal 100-kΩ pulldown resistors on the SOP lines). An external 10-kΩ pullup resistor is required to pull these pins high. See Section 5.11 for SOP[2:0] configuration modes. |
| Reset | RESET input for the device | | Never leave the reset pin floating |
| JTAG | JTAG interface | | Leave as NC if unused |

# 4. Specifications

All measurements are referenced at the module pins unless otherwise indicated. All specifications are over process and voltage unless otherwise indicated.
Over operating free-air temperature range (unless otherwise noted)[1] [2]

## 4.1 Absolute Maximum Ratings

**Table 4-1. Absolute Maximum Ratings**

| PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{BAT}$ | –0.5 | 3.8 | V |
| Digital I/O | –0.5 | $V_{BAT}$ + 0.5 | V |
| Analog pins | –0.5 | 2.1 | V |
| Operating temperature ($T_A$) | –40 | 85 | °C |
| Storage temperature ($T_{stg}$) | –40 | 85 | °C |
| Junction temperature ($T_j$)[3] | | 120 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to $V_{SS}$, unless otherwise noted.

(3) Junction temperature is for the CC3235SF device that is contained within the module.

## 4.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS001[1] | | ±2000 | V |
| | Charged device model (CDM), per JESD22-C101[2] | All pins | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 4.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted) [2] [1] [3]

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| $V_{BAT}$ | 2.3 | 3.3 | 3.6 | V |
| Operating temperature | –40 | 25 | 85 | °C |
| Ambient thermal slew | –20 | | 20 | °C/minute |

(1) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.
(2) To ensure WLAN performance, the ripple on the power supply must be less than ±300 mV. The ripple should not cause the supply to fall below the brownout voltage.
(3) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. The brownout condition is also 2.1 V, and care must be taken when operating at the minimum specified voltage.

## 4.4 Brownout and Blackout Conditions

The module enters a brownout condition whenever the input voltage dips below $V_{BROWNOUT}$ (see Figure 4-1 and Figure 4-2). This condition must be considered during design of the power supply routing, especially if operating from a battery. High-current operations, such as a TX packet or any external activity (not necessarily related directly to networking) can cause a drop in the supply voltage, potentially triggering a brownout. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (four contacts for a 2× AA battery), and the wiring and PCB routing resistance.

**Note**

When the module is in HIBERNATE state, brownout is not detected. Only blackout is in effect during HIBERNATE state.

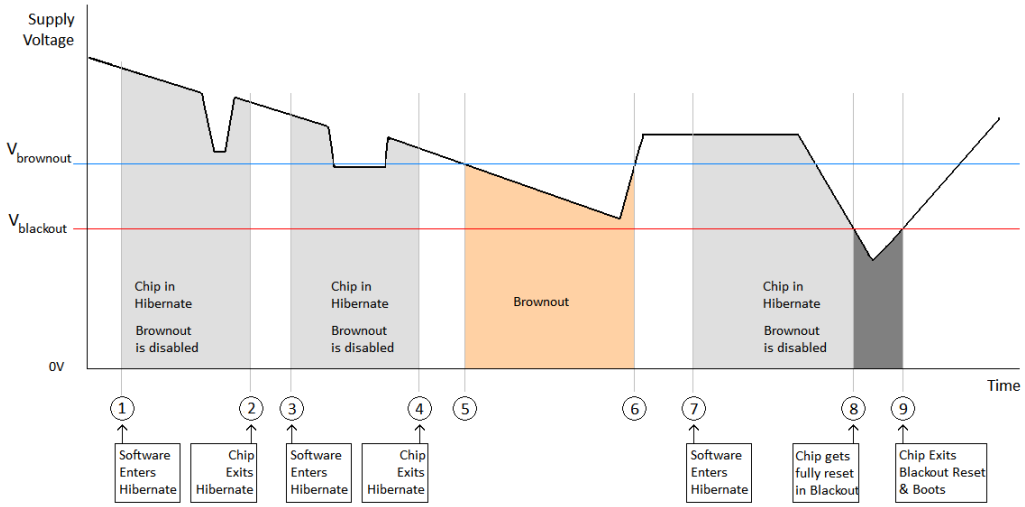


**Figure 4-1. Brownout and Blackout Levels (1 of 2)**

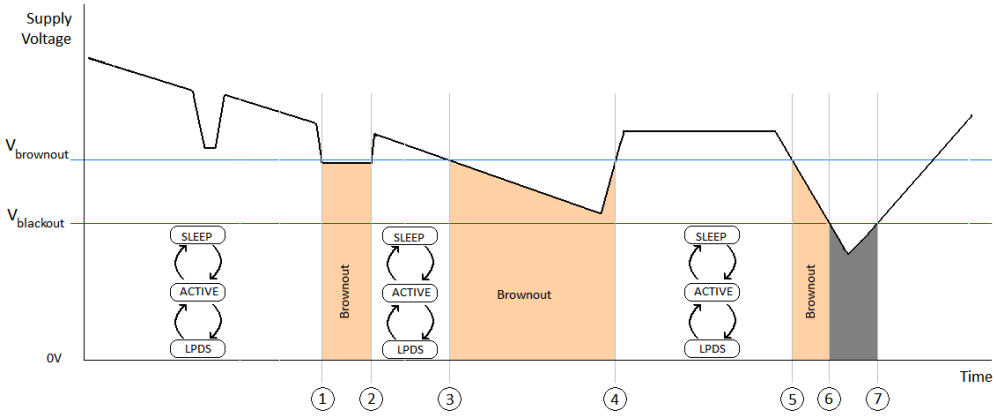


**Figure 4-2. Brownout and Blackout Levels (2 of 2)**

In the brownout condition, all sections of the device shut down within the module except for the Hibernate block (including the 32-kHz RTC clock), which remains on. The current in this state can reach approximately 400 µA.

The blackout condition is equivalent to a hardware reset event in which all states within the module are lost. $V_{brownout}$ = 2.1 V and $V_{blackout}$ = 1.67 V

Table 4-2 lists the brownout and blackout voltage levels.

**Table 4-2. Brownout and Blackout Voltage Levels**

| CONDITION | VOLTAGE LEVEL | UNIT |
|---|---|---|
| $V_{brownout}$ | 2.1 | V |
| $V_{blackout}$ | 1.67 | V |

## 4.5 Electrical Characteristics for GPIO Pins

**Table 4-3. GPIO Pins Except 25, 26, 42, and 44 (25°C) (1)**

$T_A$ = 25°C, $V_{BAT}$ = 3.3 V

| PARAMETER | | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Pin capacitance | | | | 4 | | pF |
| $V_{IH}$ | High-level input voltage | | | 0.65 × $V_{DD}$ | | $V_{DD}$ + 0.5 V | V |
| $V_{IL}$ | Low-level input voltage | | | –0.5 | | 0.35 × $V_{DD}$ | V |
| $I_{IH}$ | High-level input current | | | | 5 | | nA |
| $I_{IL}$ | Low-level input current | | | | 5 | | nA |
| $V_{OH}$ | High-level output voltage | | IL = 2 mA; configured I/O drive strength = 2 mA; | | | $V_{DD}$ × 0.8 | V |
| | | | IL = 4 mA; configured I/O drive strength = 4 mA; | | | $V_{DD}$ × 0.7 | |
| | | | IL = 6 mA; configured I/O drive strength = 6 mA; | | | $V_{DD}$ × 0.7 | |
| | | | IL = 2 mA; configured I/O drive strength = 2 mA; | | | $V_{DD}$ × 0.75 | |
| $V_{OL}$ | Low-level output voltage | | IL = 2 mA; configured I/O drive strength = 2 mA; | $V_{DD}$ × 0.2 | | | V |
| | | | IL = 4 mA; configured I/O drive strength = 4 mA; | $V_{DD}$ × 0.2 | | | |
| | | | IL = 6 mA; configured I/O drive strength = 6 mA; | $V_{DD}$ × 0.2 | | | |
| | | | IL = 2 mA; configured I/O drive strength = 2 mA; | $V_{DD}$ × 0.25 | | | |
| $I_{OH}$ | High-level source current | 2-mA drive | | 2 | | | mA |
| | | 4-mA drive | | 4 | | | |
| | | 6-mA drive | | 6 | | | |
| $I_{OL}$ | Low-level sink current | 2-mA drive | | 2 | | | mA |
| | | 4-mA drive | | 4 | | | |
| | | 6-mA drive | | 6 | | | |

(1) We recommend using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

**Table 4-4. GPIO Pins 25, 26, 42, and 44 (25°C) (1)**

| PARAMETER | | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Pin capacitance | | | | 7 | | p |
| $V_{IH}$ | High-level input voltage | | | 0.65 × $V_{DD}$ | | $V_{DD}$ + 0.5 V | V |
| $V_{IL}$ | Low-level input voltage | | | –0.5 | | 0.35 × $V_{DD}$ | V |
| $I_{IH}$ | High-level input current | | | | 50 | | nA |
| $I_{IL}$ | Low-level input current | | | | 50 | | nA |
| $V_{OH}$ | High-level output voltage | | IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ $V_{DD}$ < 3.6 V | | | $V_{DD}$ × 0.8 | V |
| | | | IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ $V_{DD}$ < 3.6 V | | | $V_{DD}$ × 0.7 | |
| | | | IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ $V_{DD}$ < 3.6 V | | | $V_{DD}$ × 0.7 | |
| | | | IL = 2 mA; configured I/O drive strength = 2 mA; 2.3 V ≤ $V_{DD}$ < 2.4 V | | | $V_{DD}$ × 0.75 | |
| $V_{OL}$ | Low-level output voltage | | IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ $V_{DD}$ < 3.6 V | $V_{DD}$ × 0.2 | | | V |
| | | | IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ $V_{DD}$ < 3.6 V | $V_{DD}$ × 0.2 | | | |
| | | | IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ $V_{DD}$ < 3.6 V | $V_{DD}$ × 0.2 | | | |
| | | | IL = 2 mA; configured I/O drive strength = 2 mA; 2.3 V ≤ $V_{DD}$ < 2.4 V | $V_{DD}$ × 0.25 | | | |
| $I_{OH}$ | High-level source current, $V_{OH}$ = 2.4 | 2-mA drive | | 1.5 | | | mA |
| | | 4-mA drive | | 2.5 | | | |
| | | 6-mA drive | | 3.5 | | | |
| $I_{OL}$ | Low-level sink current | 2-mA drive | | 1.5 | | | mA |
| | | 4-mA drive | | 2.5 | | | |
| | | 6-mA drive | | 3.5 | | | |
| $V_{IL}$ | nRESET | | | | 0.6 | | V |

(1) We recommend using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

### 4.5.1 Electrical Characteristics for Pin Internal Pullup and Pulldown (25°C)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{OH}$ | Pullup current ($V_{DD}$ = 3.0 V) | | | 10 | | µA |
| $I_{OL}$ | Pulldown current ($V_{DD}$ = 3.0 V) | | | 10 | | µA |

## 4.6 BLE and WLAN Coexistence Requirements

For proper BLE and WLAN 2.4 GHz radio coexistence, the following requirements must be met:

**Table 4-5. BLE/WLAN Coex Isolation Requirement**

| PARAMETER | Band | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Port-to-port isolation | Dual antenna configuration(1) | 20(2) | | | dB |

(1) A single antenna configuration is possible using the CC3x35 devices.

(2) For dual antenna configuration, the antenna placement must be such that isolation between the BLE and WLAN ports is at least 20 dB.

## 4.7 Reset Requirement

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IH}$ | Operation mode level | | 0.65 × $V_{BAT}$ | | V |
| $V_{IL}$ | Shutdown mode level(1) | 0 | 0.6 | | V |
| | Minimum time for nReset low for resetting the module | 5 | | | ms |
| $T_r$ and $T_f$ | Rise and fall times | | 20 | | µs |

(1) The nRESET pin must be held below 0.6 V for the module to register a reset.

## 4.8Timing and Switching Characteristics

### 4.8.1 Power-Up Sequencing

For proper start-up of the BDE-WF3235SFA module, perform the recommended power-up sequencing as follows:

1. Tie $V_{BAT1}$ (pin 37) and $V_{BAT2}$ (pin 40) together on the board.
2. Hold the nRESET pin low while the supplies are ramping up.

Figure 4-3 shows the reset timing diagram for the first-time power-up and reset removal.

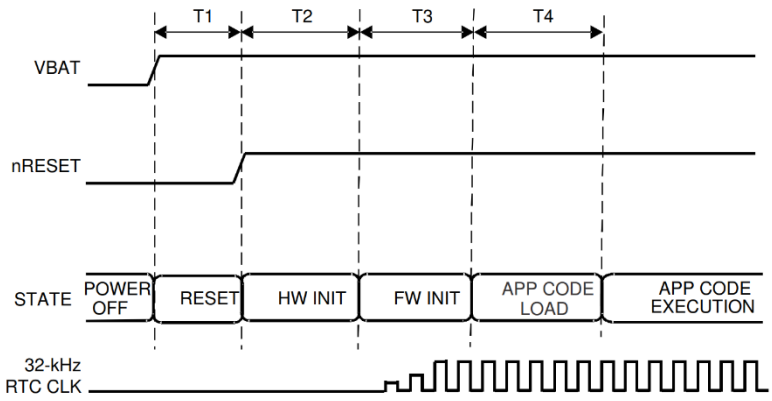


**Figure 4-3. First-Time Power-Up and Reset Removal Timing Diagram**

Table 4-6 lists the timing requirements for the first-time power-up and reset removal.

**Table 4-6. First-Time Power-Up and Reset Removal Timing Requirements**

| ITEM | NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| T1 | nReset time | nReset timing after VBAT supplies are stable | | 1 | | ms |
| T2 | Hardware wake-up time | | | 25 | | ms |
| T3 | Time taken by ROM firmware to initialize hardware | Includes internal 32-kHz XOSC settling time | | 1.1 | | s |
| T4 | App code load time for BDE-WF3235SFA | BDE-WF3235SFA | Image size (KB) × 0.06 | | | ms |

### 4.8.2 Power-Down Sequencing

For proper power down of the BDE-WF3235SFA module, ensure that the nRESET (pin 35) and nHIB (pin 4) pins have remained in a known state for a minimum of 200 ms before removing power from the module.

### 4.8.3 Device Reset

When a device restart is required, issue a negative pulse to the nRESET pin. Ensure the reset is properly applied: A negative reset pulse (on pin 35) of at least 200-mS duration.

### 4.8.4 Wake Up From Hibernate Timing

Table 4-7 lists the software hibernate timing requirements.

**Note**

The internal 32.768-kHz crystal is kept enabled by default when the module goes to hibernate.

**Table 4-7. Software Hibernate Timing Requirements**

| ITEM | NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{HIB_MIN}$ | Minimum hibernate time | | 10 | | | ms |
| $T_{wake_from_hib}$(1) | Hardware wakeup time plus firmware initialization time | | | 50(2) | | ms |
| T_APP_CODE_LOAD | App code load time for BDE-WF3235SFA | BDE-WF3235SFA | | Image size (KB) × 0.06 | | ms |

(1) $T_{wake_from_hib}$ can be 200ms on rare occasions when calibration is performed. Calibration is performed sparingly, typically when exiting Hibernate and only if temperature has changed by more than 20°C or more than 24 hours have elapsed since a prior calibration.

(2) Wake-up time can extend to 75ms if a patch is downloaded from the serial flash.

Figure 4-4 shows the timing diagram for wake up from the hibernate state.

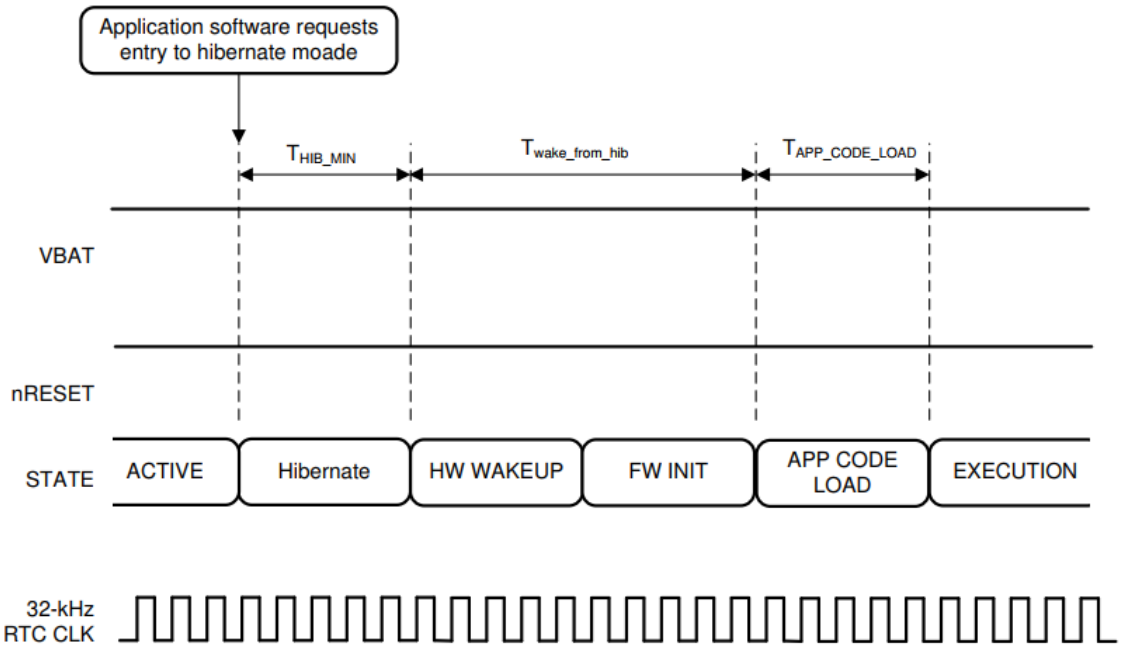


**Figure 4-4. Wake Up From Hibernate Timing Diagram**

### 4.8.5 Peripherals Timing

This section describes the peripherals that are supported by the BDE-WF3235SFA module, as follows:

- SPI
- $I^2S$
- GPIOs
- $I^2C$
- IEEE 1149.1 JTAG
- ADC
- Camera parallel port
- External flash
- UART
- SD Host
- Timers

#### 4.8.5.1 SPI

➢ SPI Master

The BDE-WF3235SFA MCU includes one SPI module, which can be configured as a master or slave device. The SPI includes a serial clock with programmable frequency, polarity, and phase; a programmable timing control between chip select and external clock generation; and a programmable delay before the first SPI word is transmitted. Slave mode does not include a dead cycle between two successive words.

Figure 4-5 shows the timing diagram for the SPI master.

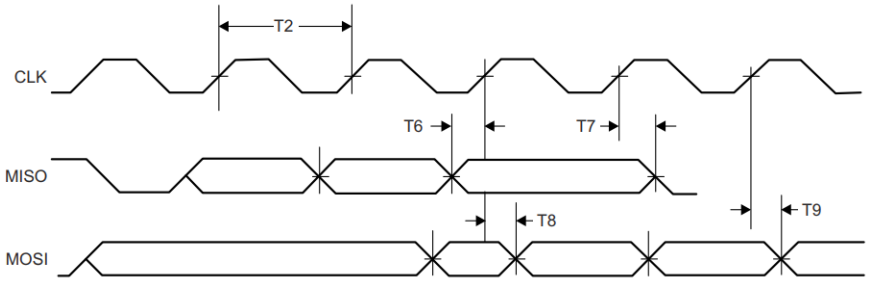


**Figure 4-5. SPI Master Timing Diagram**

Table 4-8 lists the timing parameters for the SPI master.

**Table 4-8. SPI Master Timing Parameters**

| ITEM | NAME | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | $F^{(1)}$ | Clock frequency | | 20 | MHz |
| T2 | $T_{clk}^{(1)}$ | Clock period | 50 | | ns |
| | $D^{(1)}$ | Duty cycle | 45% | 55% | |
| T6 | $t_{IS}^{(1)}$ | RX data setup time | 1 | | ns |
| T7 | $t_{IH}^{(1)}$ | RX data hold time | 2 | | ns |
| T8 | $t_{OD}^{(1)}$ | TX data output delay | | 8.5 | ns |
| T9 | $t_{OH}^{(1)}$ | TX data hold time | | 8 | ns |

(1) Timing parameter assumes a maximum load of 20 pF.

➢ SPI Slave

Figure 4-6 shows the timing diagram for the SPI slave.

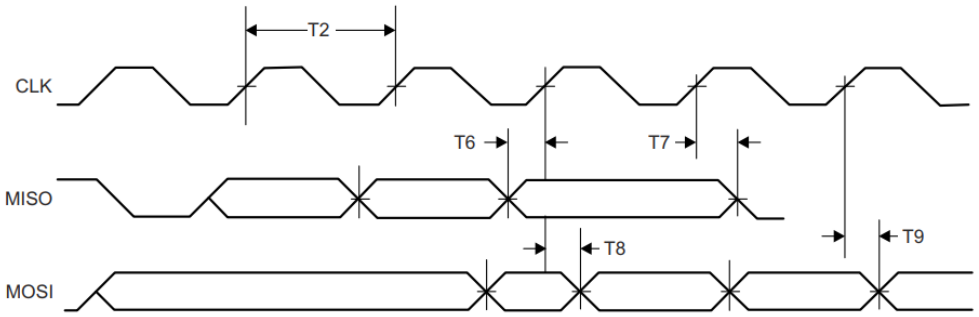


**Figure 4-6. SPI Slave Timing Diagram**

Table 4-9 lists the timing parameters for the SPI slave.

**Table 4-9. SPI Slave Timing Parameters**

| ITEM | NAME | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | $F^{(1)}$ | Clock frequency @ VBAT = 3.3 V | | 20 | MHz |
| | | Clock frequency @ VBAT ≤ 2.3 V | | 12 | |
| T2 | $T_{clk}^{(1)}$ | Clock period | 50 | | ns |
| | $D^{(1)}$ | Duty cycle | 45% | 55% | |
| T6 | $t_{IS}^{(1)}$ | RX data setup time | 4 | | ns |
| T7 | $t_{IH}^{(1)}$ | RX data hold time | 4 | | ns |
| T8 | $t_{OD}^{(1)}$ | TX data output delay | | 20 | ns |
| T9 | $t_{OH}^{(1)}$ | TX data hold time | | 24 | ns |

(1) Timing parameter assumes a maximum load of 20pF at 3.3V.

#### 4.8.5.2 I2S

The McASP interface functions as a general-purpose audio serial port optimized for multichannel audio applications and supports transfer of two stereo channels over two data pins. The McASP consists of transmit and receive sections that operate synchronously and have programmable clock and frame-sync polarity. A fractional divider is available for bit-clock generation.

- **I2S Transmit Mode**

Figure 4-7 shows the timing diagram for the I2S transmit mode.

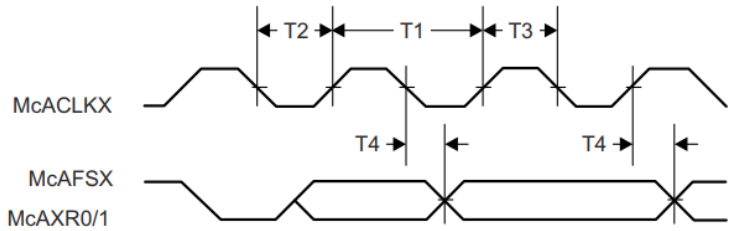


**Figure 4-7. I2S Transmit Mode Timing Diagram**

Table 4-10 lists the timing parameters for the I2S transmit mode.

**Table 4-10. I2S Transmit Mode Timing Parameters**

| ITEM | NAME | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| T1 | $f_{clk}$ (1) | Clock frequency | | 9.216 | MHz |
| T2 | $t_{LP}$ (1) | Clock low period | | 1/2 fclk | ns |
| T3 | $t_{HT}$ (1) | Clock high period | | 1/2 fclk | ns |
| T4 | $t_{OH}$ (1) | TX data hold time | | 22 | ns |

(1) Timing parameter assumes a maximum load of 20 pF.

- **I2S Receive Mode**

Figure 4-8 shows the timing diagram for the I2S receive mode.

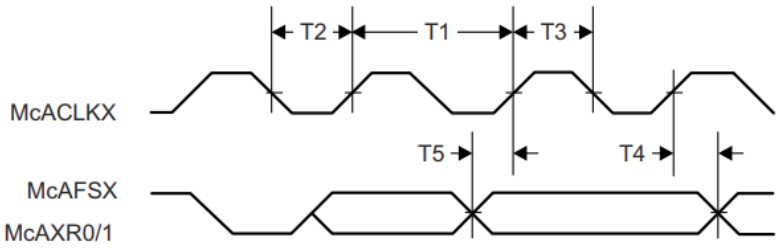


**Figure 4-8. I2S Receive Mode Timing Diagram**

Table 4-11 lists the timing parameters for the I2S receive mode.

**Table 4-11. I2S Receive Mode Timing Parameters**

| ITEM | NAME | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| T1 | $f_{clk}$ (1) | Clock frequency | | 9.216 | MHz |
| T2 | $t_{LP}$ (1) | Clock low period | | 1/2 $f_{clk}$ | ns |
| T3 | $t_{HT}$ (1) | Clock high period | | 1/2 $f_{clk}$ | ns |
| T4 | $t_{OH}$ (1) | RX data hold time | | 0 | ns |
| T5 | $t_{OS}$ (1) | RX data setup time | | 15 | ns |

(1) Timing parameter assumes a maximum load of 20 pF.

#### 4.8.5.3 GPIOs

All digital pins of the module can be used as general-purpose input/output (GPIO) pins. The GPIO module consists of four GPIO blocks, each of which provides eight GPIOs. The GPIO module supports 24 programmable GPIO pins, depending on the peripheral used. Each GPIO has configurable pullup and pulldown strength (weak 10 µA), configurable drive strength (2, 4, and 6 mA), and open-drain enable.

Figure 4-9 shows the GPIO timing diagram.

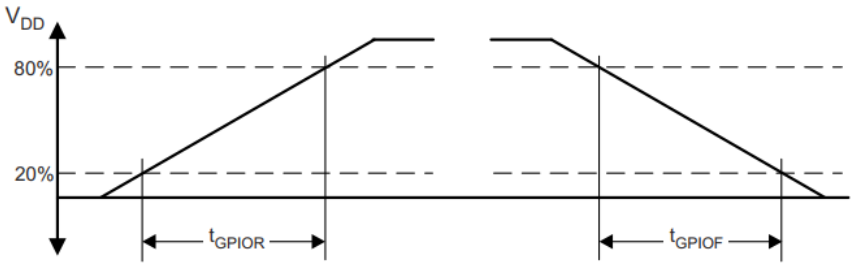


**Figure 4-9. GPIO Timing Diagram**

Table 4-12 lists the GPIO output transition times for $V_{BAT}$ = 2.3 V.

**Table 4-12. GPIO Output Transition Times (VBAT = 2.3 V)(1) (2)**

| DRIVE STRENGTH (mA) | DRIVE STRENGTH CONTROL BITS | $T_r$ | | | $T_f$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| 2 | 2MA_EN=1<br>4MA_EN=0 | 11.7 | 13.9 | 16.3 | 11.5 | 13.9 | 16.7 | ns |
| 4 | 2MA_EN=0<br>4MA_EN=1 | 13.7 | 15.6 | 18.0 | 9.9 | 11.6 | 13.6 | ns |
| 6 | 2MA_EN=1<br>4MA_EN=1 | 5.5 | 6.4 | 7.4 | 3.8 | 4.7 | 5.8 | ns |

(1) $V_{BAT}$ = 2.3 V, T = 25°C, total pin load = 30 pF
(2) The transition data applies to the pins other than the multiplexed analog-digital pins 25, 26, 42, and 44.

Table 4-13 lists the GPIO output transition times for $V_{BAT}$ = 3.3 V.

**Table 4-13. GPIO Output Transition Times (VBAT = 3.3 V)(1) (2)**

| DRIVE STRENGTH (mA) | DRIVE STRENGTH CONTROL BITS | $T_r$ | | | $T_f$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| 2 | 2MA_EN=1<br>4MA_EN=0 | 8.0 | 9.3 | 10.7 | 8.2 | 9.5 | 11.0 | ns |
| 4 | 2MA_EN=0<br>4MA_EN=1 | 6.6 | 7.1 | 7.6 | 4.7 | 5.2 | 5.8 | ns |
| 6 | 2MA_EN=1<br>4MA_EN=1 | 3.2 | 3.5 | 3.7 | 2.3 | 2.6 | 2.9 | ns |

(1) $V_{BAT}$ = 3.3 V, T = 25°C, total pin load = 30 pF
(2) The transition data applies to the pins except the multiplexed analog-digital pins 29, 30, 45, 50, 52 and 53.

Table 4-14 lists the input transition time parameters.

**Table 4-14. GPIO Input Transition Time Parameters**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_r$ | Input transition time ($t_r$, $t_f$), 10% to 90% | 1 | 3 | ns |
| $t_f$ | | 1 | 3 | ns |

### 4.8.5.4 I²C

The BDE-WF3235SFA MCU includes one I²C module operating with standard (100 kbps) or fast (400 kbps) transmission speeds.

Figure 4-10 shows the I²C timing diagram.

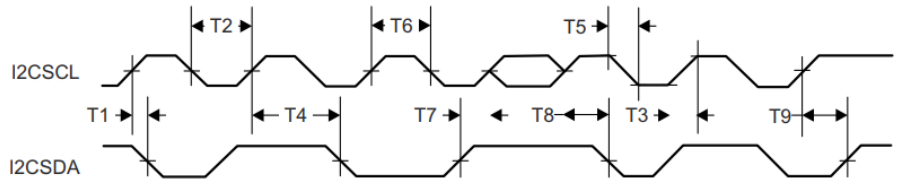


**Figure 4-10. I²C Timing Diagram**

Table 4-15 lists the I²C timing parameters.

**Table 4-15. I²C Timing Parameters(3)**

| ITEM | NAME | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| T2 | $t_{LP}$ | Clock low period | See (1) | | System clock |
| T3 | $t_{SRT}$ | SCL/SDA rise time | | See (2) | ns |
| T4 | $t_{DH}$ | Data hold time | NA | | |
| T5 | $t_{SFT}$ | SCL/SDA fall time | 3 | | ns |
| T6 | $t_{HT}$ | Clock high time | See (1) | | System clock |
| T7 | $t_{DS}$ | Data setup time | tLP/2 | | System clock |
| T8 | $t_{SCSR}$ | Start condition setup time | 36 | | System clock |
| T9 | $t_{SCS}$ | Stop condition setup time | 24 | | System clock |

(1) This value depends on the value programmed in the clock period register of I²C. Maximum output frequency is the result of the minimal value programmed in this register.

(2) Because I²C is an open-drain interface, the controller can drive logic 0 only. Logic is the result of external pullup. Rise time depends on the value of the external signal capacitance and external pullup register.

(3) All timing is with 6-mA drive and 20-pF load.

#### 4.8.5.5 IEEE 1149.1 JTAG

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see the IEEE Standard 1149.1,*Test Access Port and Boundary-Scan Architecture*.

Figure 4-11 shows the JTAG timing diagram.

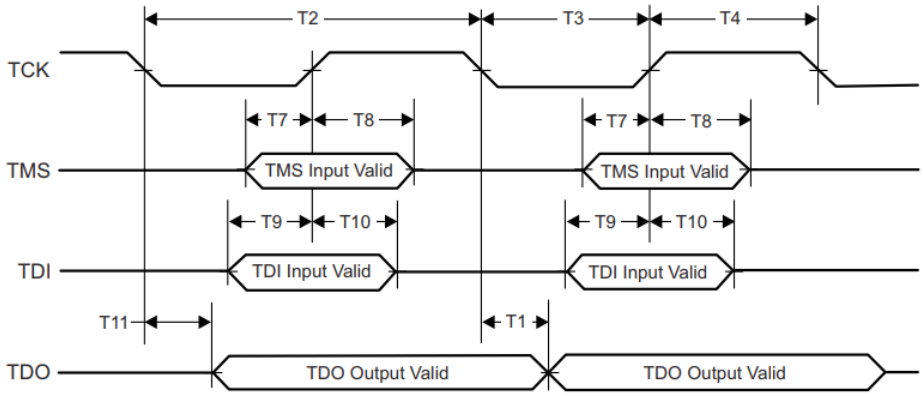


**Figure 4-11. JTAG Timing Diagram**

Table 4-16 lists the JTAG timing parameters.

**Table 4-16. JTAG Timing Parameters**

| ITEM | NAME | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| T1 | $f_{TCK}$ | Clock frequency | | 15 | MHz |
| T2 | $t_{TCK}$ | Clock period | | 1 / $f_{TCK}$ | ns |
| T3 | $t_{CL}$ | Clock low period | | $t_{TCK}$ / 2 | ns |
| T4 | $t_{CH}$ | Clock high period | | $t_{TCK}$ / 2 | ns |
| T7 | $t_{TMS_SU}$ | TMS setup time | 1 | | ns |
| T8 | $t_{TMS_HO}$ | TMS hold time | 16 | | ns |
| T9 | $t_{TDI_SU}$ | TDI setup time | 1 | | ns |
| T10 | $t_{TDI_HO}$ | TDI hold time | 16 | | ns |
| T11 | $t_{TDO_HO}$ | TDO hold time | | 15 | ns |

#### 4.8.5.6 ADC

Table 4-17 lists the ADC electrical specifications. See *CC32xx ADC Appnote* for further information on using the ADC and for application-specific examples.

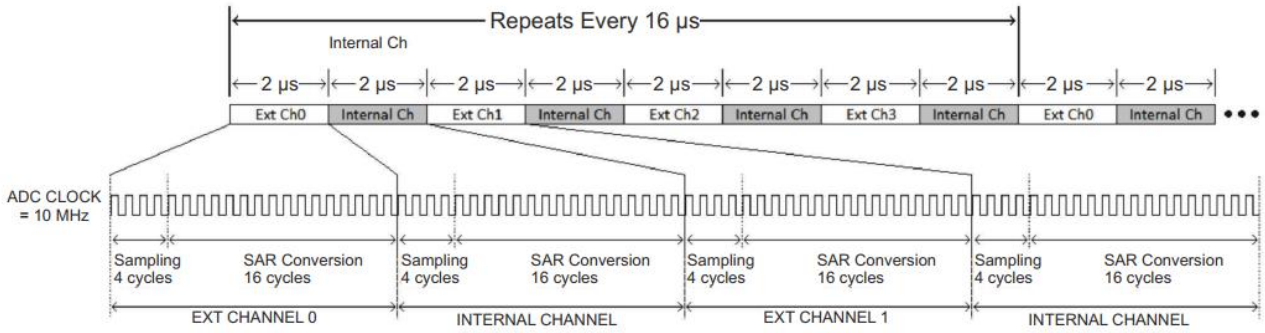


**Figure 4-12. ADC Clock Timing Diagram**

Figure 4-12 shows the ADC clock timing diagram.

**Table 4-17. ADC Electrical Specifications**

| PARAMETER | DESCRIPTION | TEST CONDITIONS / ASSUMPTIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Nbits | Number of bits | | | 12 | | Bits |
| INL | Integral nonlinearity | Worst-case deviation from histogram method over full scale (not including first and last three LSB levels) | –2.5 | | 2.5 | LSB |
| DNL | Differential nonlinearity | Worst-case deviation of any step from ideal | –1 | | 4 | LSB |
| Input range | | | 0 | | 1.4 | V |
| Driving source impedance | | | | | 100 | Ω |
| FCLK | Clock rate | Successive approximation input clock rate | | 10 | | MHz |
| Input capacitance | | | | 12 | | pF |
| Input impedance | | ADC Pin 57 | | 2.15 | | kΩ |
| | | ADC Pin 58 | | 0.7 | | |
| | | ADC Pin 59 | | 2.12 | | |
| | | ADC Pin 60 | | 1.17 | | |
| Number of channels | | | | 4 | | |
| $F_{sample}$ | Sampling rate of each pin | | | 62.5 | | KSPS |
| F_input_max | Maximum input signal frequency | | | | 31 | kHz |
| SINAD | Signal-to-noise and distortion | Input frequency DC to 300 Hz and 1.4 $V_{pp}$ sine wave input | 55 | 60 | | dB |
| I_active | Active supply current | Average for analog-to-digital during conversion without reference current | | 1.5 | | mA |
| I_PD | Power-down supply current for core supply | Total for analog-to-digital when not active (this must be the SoC level test) | | 1 | | µA |

| | | | | |
|---|---|---|---|---|
| Absolute offset error | | FCLK = 10 MHz | ±2 | mV |

**Table 4-17. ADC Electrical Specifications (continued)**

| PARAMETER | DESCRIPTION | TEST CONDITIONS / | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Gain error | | | | ±2% | | |
| $V_{ref}$ | ADC reference voltage | | | 1.467 | | V |

### 4.8.5.7 Camera Parallel Port

The fast camera parallel port interfaces with a variety of external image sensors, stores the image data in a FIFO, and generates DMA requests. The camera parallel port supports 8 bits.

Figure 4-13 shows the timing diagram for the camera parallel port.

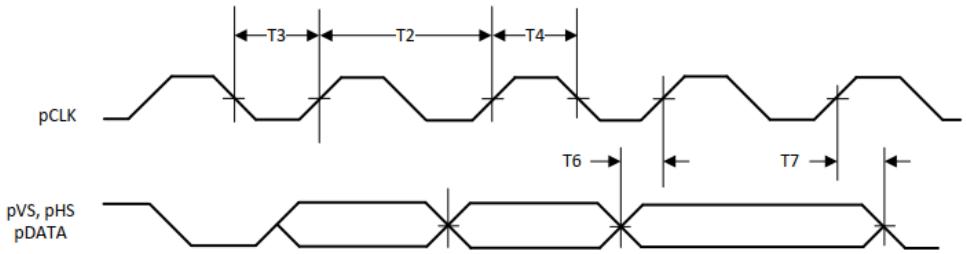


**Figure 4-13. Camera Parallel Port Timing Diagram**

Table 4-18 lists the timing parameters for the camera parallel port.

**Table 4-18. Camera Parallel Port Timing Parameters**

| ITEM | NAME | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | pCLK | Clock frequency | | 2 | MHz |
| T2 | $T_{clk}$ | Clock period | | 1/pCLK | ns |
| T3 | $t_{LP}$ | Clock low period | | $T_{clk}/2$ | ns |
| T4 | $t_{HT}$ | Clock high period | | $T_{clk}/2$ | ns |
| T6 | $t_{IS}$ | RX data setup time | | 2 | ns |
| T7 | $t_{IH}$ | RX data hold time | | 2 | ns |

### 4.8.5.8 UART

The BDE-WF3235SFA MCU includes two UARTs with the following features:

- Programmable baud-rate generator allowing speeds up to 3 Mbps
- Separate 16-bit × 8-bit TX and RX FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including a 1-byte-deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Generation and detection of line-breaks
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 data bits
  - Generation and detection of even, odd, stick, or no-parity bits
  - Generation of 1 or 2 stop-bits
- RTS and CTS hardware flow support
- Standard FIFO-level and end-of-transmission interrupts
- Efficient transfers using µDMA:
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level
- System clock is used to generate the baud clock.

#### 4.8.5.9 External Flash Interface

The BDE-WF3235SFA MCU includes the Macronix™ 32-Mbit serial flash. The serial flash can be programmed directly using the external flash interface (pins 13, 14, 15, and 17). During normal operation, the external flash interface should remain unconnected.

For timing details, see the MX25R3235F data sheet.

#### 4.8.5.10 SD Host

The BDE-WF3235SFA MCU provides an interface between a local host (LH), such as an MCU and an SD memory card, and handles SD transactions with minimal LH intervention.

The SD host does the following:

- Provides SD card access in 1-bit mode
- Deals with SD protocol at the transmission level
- Handles data packing
- Adds cyclic redundancy checks (CRC)
- Start and end bit
- Checks for syntactical correctness

The application interface sends every SD command and either polls for the status of the adapter or waits for an interrupt request. The result is then sent back to the application interface in case of exceptions or to warn of end-of-operation. The controller can be configured to generate DMA requests and work with minimum CPU intervention. Given the nature of integration of this peripheral on the CC3235x platform, we recommend that developers use peripheral library APIs to control and operate the block. This section emphasizes understanding the SD host APIs provided in the peripheral library of the CC3235x Software Development Kit (SDK).

The SD host features are as follows:

- Full compliance with SD command and response sets, as defined in the SD memory card
  - Specifications, v2.0
  - Includes high-capacity (size >2 GB) cards HC SD
- Flexible architecture, allowing support for new command structure.
- 1-bit transfer mode specifications for SD cards
- Built-in 1024-byte buffer for read or write
  - 512-byte buffer for both transmit and receive
  - Each buffer is 32-bits wide by 128-words deep
- 32-bit-wide access bus to maximize bus throughput
- Single interrupt line for multiple interrupt source events
- Two slave DMA channels (1 for TX, 1 for RX)
- Programmable clock generation
- Integrates an internal transceiver that allows a direct connection to the SD card without external transceiver
- Supports configurable busy and response timeout
- Support for a wide range of card clock frequency with odd and even clock ratio
- Maximum frequency supported is 24 MHz

#### 4.8.5.11 Timers

Programmable timers can be used to count or time external events that drive the timer input pins. The general-purpose timer module (GPTM) of the BDE-WF3235SFA MCU contains 16- or 32-bit GPTM blocks. Each 16- or 32-bit GPTM block provides two 16-bit timers or counters (referred to as Timer A and Timer B) that can be configured to operate independently as timers or event counters, or they can be concatenated to operate as one 32-bit timer. Timers can also be used to trigger µDMA transfers.

The GPTM contains four 16- or 32-bit GPTM blocks with the following functional options:

- Operating modes:
  - 16- or 32-bit programmable one-shot timer
  - 16- or 32-bit programmable periodic timer
  - 16-bit general-purpose timer with an 8-bit prescaler
  - 16-bit input-edge count- or time-capture modes with an 8-bit prescaler
  - 16-bit PWM mode with an 8-bit prescaler and software-programmable output inversion of the PWM signal
- Counts up or counts down
- Sixteen 16- or 32-bit capture compare pins (CCP)
- User-enabled stalling when the microcontroller asserts CPU Halt flag during debug
- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the interrupt service routine
- Efficient transfers using micro direct memory access controller (µDMA):
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt
- Runs from system clock (80 MHz)

# 5. Detailed Description

## 5.1 Overview

The BDE-WF3235SFA MCU is a Dual-Band Wi-Fi internet-on-a chip module that consists of an Arm Cortex-M4 processor with a rich set of peripherals for diverse application requirements, a Wi-Fi network processor, and power-management subsystems.

## 5.2 Functional Block Diagram

Figure 5-1 shows the functional block diagram of the BDE-WF3235SFA solution.

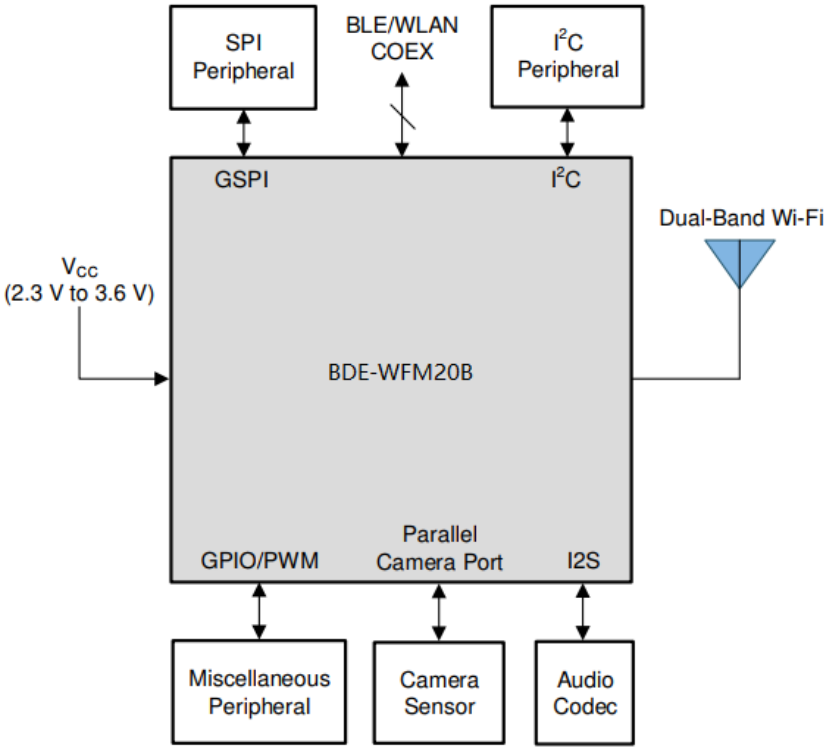


**Figure 5-1. Functional Block Diagram**

## 5.3 Arm Cortex-M4 Processor Core Subsystem

The high-performance Arm Cortex-M4 processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- The Cortex-M4 core has low-latency interrupt processing with the following features:
  - A 32-bit Arm Thumb® instruction set optimized for embedded applications
  - Handler and thread modes
  - Low-latency interrupt handling by automatic processor state saving and restoration during entry and exit
  - Support for ARMv6 unaligned accesses
- Nested vectored interrupt controller (NVIC) closely integrated with the processor core to achieve low-latency interrupt processing. The NVIC includes the following features:
  - Bits of priority configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping that enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
  - Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead
  - Wake-up interrupt controller (WIC) providing ultra-low-power sleep mode support
- Bus interfaces:
  - Advanced high-performance bus (AHB-Lite) interfaces: system bus interfaces
  - Bit-band support for memory and select peripheral that includes atomic bit-band write and read operations
- Low-cost debug solution featuring:
  - Debug access to all memory and registers in the system, including access to memory-mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted
  - Serial wire debug port (SW-DP) or serial wire JTAG debug port (SWJ-DP) debug access
  - Flash patch and breakpoint (FPB) unit to implement breakpoints and code patches

## 5.4 Wi-Fi Network Processor Subsystem

The Wi-Fi network processor subsystem includes a dedicated Arm MCU to completely offload the host MCU along with an 802.11 a/b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The BDE-WF3235SFA MCU supports station, AP, and Wi-Fi Direct modes. The module also supports WPA2 personal and enterprise security, WPS 2.0, and WPA3 personal [1]. The Wi-Fi network processor includes an embedded IPv6, IPv4 TCP/IP stack, TLS stack, and network applications such as HTTPS server.

### 5.4.1 WLAN

The WLAN features are as follows:

- 802.11 a/b/g/n integrated radio, modem, and MAC supporting WLAN communication as a BSS station, AP, Wi-Fi Direct client and group owner with CCK and OFDM rates in the 2.4 GHz ISM band, channels 1 to 13, and 5 GHz U-NII band.

**Note**

802.11n is supported only in Wi-Fi station, Wi-Fi Direct, and P2P client modes.

- Autocalibrated radio with a single-ended 50-Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with multiple user-configurable profiles stored in serial-flash allows automatic fast connection to an access point without user or host intervention.
- Supports all common Wi-Fi security modes for personal and enterprise networks with on-chip security accelerators, including: WEP, WPA/WPA2 PSK, WPA2 Enterprise (802.1x), WPA3 Personal .
- Smart provisioning options deeply integrated within the module providing a comprehensive end-to-end solution. With elaborate events notification to the host, enabling the application to control the provisioning decision flow. The wide variety of Wi-Fi provisioning methods include:
  - Access Point using HTTPS
  - SmartConfig Technology: a 1-step, 1-time process to connect a BDE-WF3235SFA-enabled module to the home wireless network, removing dependency on the I/O capabilities of the host MCU; thus, it is usable by deeply embedded applications
- 802.11 transceiver mode allows transmitting and receiving of proprietary data through a socket without adding MAC or PHY headers. The 802.11 transceiver mode provides the option to select the working channel, rate, and transmitted power. The receiver mode works with the filtering options.

### 5.4.2 Network Stack

The Network Stack features are as follows:

- Integrated IPv4, IPv6 TCP/IP stack with BSD socket APIs for simple Internet connectivity with any MCU, microprocessor, or ASIC

**Note**

Not all APIs are 100% BSD compliant. Not all BSD APIs are supported.

- Support of 16 simultaneous TCP, UDP, RAW, SSL\TLS sockets
- Built-in network protocols:
  - Static IP, LLA, DHCPv4, DHCPv6 with DAD and stateless autoconfiguration
  - ARP, ICMPv4, IGMP, ICMPv6, MLD, ND
  - DNS client for easy connection to the local network and the Internet

[1] See CC3x35 SDK v3.40 or newer for details. Limited to STA mode only.

- Built-in network application and utilities:
  - HTTP/HTTPS
    - Web page content stored on serial flash
    - RESTful APIs for setting and configuring application content
    - Dynamic user callbacks
  - Service discovery: Multicast DNS service discovery lets a client advertise its service without a centralized server. After connecting to the access point, the BDE-WF3235SFA MCU provides critical information, such as device name, IP, vendor, and port number.
  - DHCP server
  - Ping

Table 5-1 describes the NWP features.

**Table 5-1. NWP Features**

| Feature | Description |
|---|---|
| Wi-Fi standards | 802.11a/b/g/n station<br>802.11a/b/g AP supporting up to four stations<br>Wi-Fi Direct client and group owner |
| Wi-Fi channels | 2.4 GHz ISM and 5 GHz U-NII Channels |
| Channel Bandwidth | 20 MHz |
| Wi-Fi security | WEP, WPA/WPA2 PSK, WPA2 enterprise (802.1x), WPA3 personal(1) |
| Wi-Fi provisioning | SmartConfig technology, Wi-Fi protected setup (WPS2), AP mode with internal HTTP web server |
| IP protocols | IPv4/IPv6 |
| IP addressing | Static IP, LLA, DHCPv4, DHCPv6 with DAD |
| Cross layer | ARP, ICMPv4, IGMP, ICMPv6, MLD, NDP |
| Transport | UDP, TCP<br>SSLv3.0/TLSv1.0/TLSv1.1/TLSv1.2<br>RAW |
| Network applications and utilities | Ping<br>HTTP/HTTPS web server<br>mDNS<br>DNS-SD<br>DHCP server |
| Host interface | UART/SPI |
| Security | Device identity<br>Trusted root-certificate catalog<br>TI root-of-trust public key<br>The CC3235S and CC3235SF variants also support:<br>• Secure key storage<br>• Online certificate status protocol (OCSP)<br>• Certificate signing request (CSR)<br>• Unique per device Key-Pair<br>• File system security<br>• Software tamper detection<br>• Cloning protection<br>• Secure boot<br>• Validate the integrity and authenticity of the run-time binary during boot<br>• Initial secure programming |

**Table 5-1. NWP Features (continued)**

| Feature | Description |
|---|---|
| Power management | Enhanced power policy management uses 802.11 power save and deep-sleep power modes |
| Other | Transceiver<br>Programmable RX filters with event-trigger mechanism<br>Rx Metrics for tracking the surrounding RF |

(1) See CC3x35 SDK v3.40 or newer for details. Limited to STA mode only.

## 5.5 Security

The BDE-WF3235SFA internet-on-a chip module enhances the security capabilities available for development of IoT devices, while completely offloading these activities from the MCU to the networking subsystem. The security capabilities include the following key features:

**Wi-Fi and Internet Security:**

- Personal and enterprise Wi-Fi security
  - Personal standards
    - AES (WPA2-PSK)
    - TKIP (WPA-PSK)
    - WEP
  - Enterprise standards
    - EAP Fast
    - EAP PEAPv0/1
    - EAP PEAPv0 TLS
    - EAP PEAPv1 TLS EAP LS
    - EAP TLS
    - EAP TTLS TLS
    - EAP TTLS MSCHAPv2

- Secure sockets
  - Protocol versions: SSL v3, TLS 1.0, TLS 1.1, TLS 1.2
  - Powerful crypto engine for fast, secure Wi-Fi and internet connections with 256-bit AES encryption for TLS and SSL connections
  - Ciphers suites
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_MD5
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_CBC_SHA

- SL_SEC_MASK_TLS_RSA_WITH_AES_128_GCM_SHA256
- SL_SEC_MASK_TLS_RSA_WITH_AES_256_GCM_SHA384

- SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_128_GCM_SHA256
- SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_GCM_SHA384
- SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_GCM_SHA256
- SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_GCM_SHA384
- SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_GCM_SHA256
- SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_GCM_SHA384
- SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_CHACHA20_POLY1305_SHA256
- SL_SEC_MASK_TLS_ECDHE_RSA_WITH_CHACHA20_POLY1305_SHA256
- SL_SEC_MASK_TLS_DHE_RSA_WITH_CHACHA20_POLY1305_SHA256

  – Server authentication
  – Client authentication
  – Domain name verification
  – Runtime socket upgrade to secure socket – STARTTLS
- Secure HTTP server (HTTPS)
- Trusted root-certificate catalog – Verifies that the CA used by the application is trusted and known secure content delivery
- TI root-of-trust public key – Hardware-based mechanism that allows authenticating TI as the genuine origin of a given content using asymmetric keys
- Secure content delivery – Allows encrypted file transfer to the system using asymmetric keys created by the device

**Code and Data Security:**

- Network passwords and certificates are encrypted and signed
- Cloning protection – Application and data files are encrypted by a unique key per device
- Access control – Access to application and data files only by using a token provided in file creation time. If an unauthorized access is detected, a tamper protection lockdown mechanism takes effect
- Encrypted and authenticated file system
- Secured boot – Authentication of the application image on every boot
- Code and data encryption – User application and data files are encrypted in sFlash
- Code and data authentication – User Application and data files are authenticated with a public key certificate
- Offloaded crypto library for asymmetric keys, including the ability to create key-pair, sign and verify data buffer
- Recovery mechanism

**Device Security:**

- Separate execution environments – Application processor and network processor run on separate Arm cores
- Initial secure programming – Allows for keeping the content confidential on the production line
- Debug security
  – JTAG lock
  – Debug ports lock
- True random number generator

Figure 5-2 shows the high-level structure of the CC3235SF device that is contained within the BDE-WF3235SFA module. The application image, user data, and network information files (passwords, certificates) are encrypted

using a device-specific key.

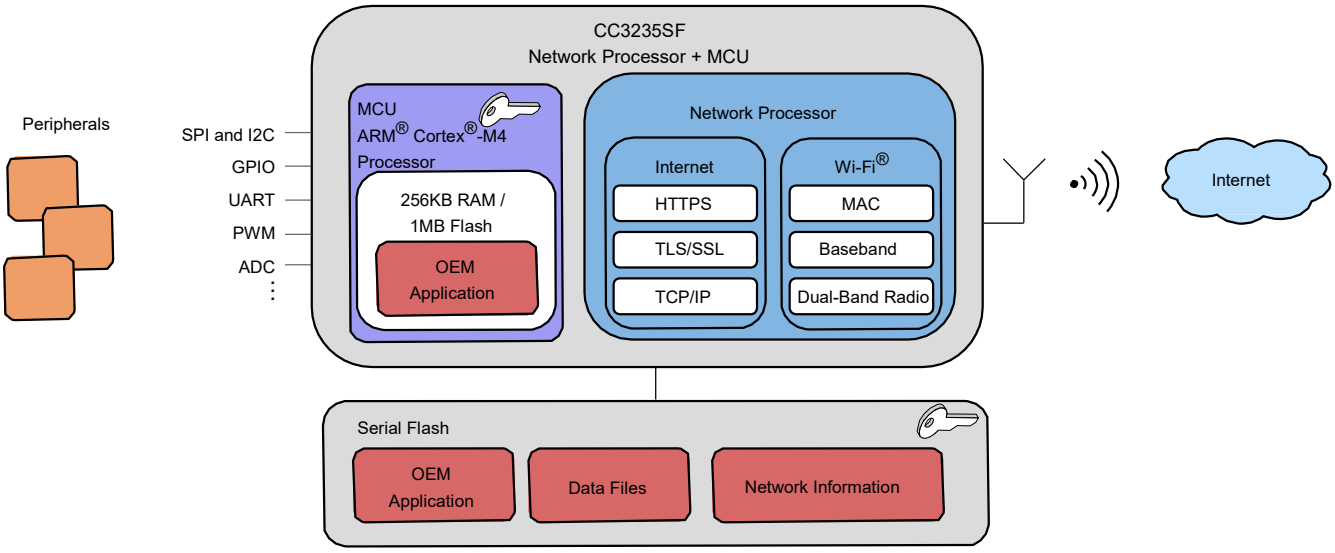


**Figure 5-2. CC3235SF High-Level Structure**

## 5.6 Power-Management Subsystem

The BDE-WF3235SFA power-management subsystem contains DC/DC converters to accommodate the differing voltage or current requirements of the system.

The BDE-WF3235SFA MCU is a fully integrated module-based WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC/DC converters and LDOs, generates all of the voltages required for the module to operate from a wide variety of input sources. For maximum flexibility, the module can operate in the modes described in the following sections.

### 5.6.1 VBAT Wide-Voltage Connection

In the wide-voltage battery connection, the module can be directly connected to two AA alkaline batteries. All other voltages required to operate the module are generated internally by the DC/DC converters. This scheme is the most common mode for the module because it supports wide-voltage operation from 2.3 to 3.6 V.

## 5.7 Low-Power Operating Mode

From a power-management perspective, the BDE-WF3235SFA MCU comprises the following two independent subsystems:

- Arm Cortex-M4 application processor subsystem
- Networking subsystem

Each subsystem operates in one of several power states.

The Arm Cortex-M4 application processor runs the user application loaded from an internal serial flash, or on-module XIP flash. The networking subsystem runs preprogrammed TCP/IP and Wi-Fi data link layer functions.

The user program controls the power state of the application processor subsystem and can be in one of the five modes described in Table 5-2.

**Table 5-2. User Program Modes**

| APPLICATION PROCESSOR (MCU) MODE(1) | DESCRIPTION |
|---|---|
| MCU active mode | MCU executing code at 80-MHz state rate. |
| MCU sleep mode | The MCU clocks are gated off in sleep mode and the entire state of the device is retained. Sleep mode offers instant wakeup. The MCU can be configured to wake up by an internal fast timer or by activity from any GPIO line or peripheral. |
| MCU LPDS mode | State information is lost and only certain MCU-specific register configurations are retained. The MCU can wake up from external events or by using an internal timer. (The wake-up time is less than 3ms.) Certain parts of memory can be retained while the MCU is in LPDS mode. The amount of memory retained is configurable. Users can choose to preserve code and the MCU-specific setting. The MCU can be configured to wake up using the RTC timer or by an external event on specific GPIOs as the wake-up source. |
| MCU hibernate mode | The lowest power mode in which all digital logic is power-gated. Only a small section of the logic directly powered by the input supply is retained. The RTC keeps running and the MCU supports wakeup from an external event or from an RTC timer expiry. Wake-up time is longer than LPDS mode at about 15 ms plus the time to load the application from serial flash, which varies according to code size. In this mode, the MCU can be configured to wake up using the RTC timer or external event on a GPIO. |
| MCU shutdown mode | The lowest power mode system-wise. All device logics are off, including the RTC. The wake-up time in this mode is longer than hibernate at about 1.1 s. To enter or exit the shutdown mode, the state of the nRESET line is changed (low to shut down, high to turn on). |

(1) Modes are listed in order of power consumption, with highest power modes listed first.

The NWP can be active or in LPDS mode and takes care of its own mode transitions. When there is no network activity, the NWP sleeps most of the time and wakes up only for beacon reception (see Table 5-3).

**Table 5-3. Networking Subsystem Modes**

| NETWORK PROCESSOR MODE | DESCRIPTION |
|---|---|
| Network active mode (processing layer 3, 2, and 1) | Transmitting or receiving IP protocol packets |
| Network active mode (processing layer 2 and 1) | Transmitting or receiving MAC management frames; IP processing not required. |
| Network active listen mode | Special power optimized active mode for receiving beacon frames (no other frames supported) |
| Network connected Idle | A composite mode that implements 802.11 infrastructure power save operation. The BDE-WF3235SFA NWPs automatically go into LPDS mode between beacons and then wakes to active listen mode to receive a beacon and determine if there is pending traffic at the AP. If not, the NWP returns to LPDS mode and the cycle repeats. |
| Network LPDS mode | Low-power state between beacons in which the state is retained by the NWP, allowing for a rapid wake up. |
| Network disabled | The network is disabled |

The operation of the application and network processor ensures that the module remains in the lowest power mode most of the time to preserve battery life.

The following examples show the use of the power modes in applications:

- A product that is continuously connected to the network in the 802.11 infrastructure power-save mode but sends and receives little data spends most of the time in connected idle, which is a composite of receiving a beacon frame and waiting for the next beacon.
- A product that is not continuously connected to the network but instead wakes up periodically (for example, every 10 minutes) to send data, spends most of the time in hibernate mode, jumping briefly to active mode to transmit data.

## 5.8 Memory

### 5.8.1 Internal Memory

The CC3235SF device within the BDE-WF3235SFA module includes on-chip SRAM to which application programs are downloaded and executed. The application developer must share the SRAM for code and data. The micro direct memory access (µDMA) controller can transfer data to and from SRAM and various peripherals. The CC3235SF device ROM holds the rich set of peripheral drivers, which saves SRAM space. For more information on drivers, see the CC3235SF API list.

#### 5.8.1.1 SRAM

The BDE-WF3235SFA MCU family provides 256KB of on-chip SRAM. Internal RAM is capable of selective retention during LPDS mode. This internal SRAM is at offset 0x2000 0000 of the device memory map.

Use the µDMA controller to transfer data to and from the SRAM.

When the device enters low-power mode, the application developer can choose to retain a section of memory based on need. Retaining the memory during low-power mode provides a faster wakeup. The application developer can choose the amount of memory to retain in multiples of 64KB. For more information, see the API guide.

#### 5.8.1.2 ROM

The internal zero-wait-state ROM of the BDE-WF3235SFA module is at address 0x0000 0000 of the device memory and is programmed with the following components:

- Bootloader
- Peripheral driver library (DriverLib) release for product-specific peripherals and interfaces

The bootloader is used as an initial program loader (when the serial flash memory is empty). The DriverLib software library of the BDE-WF3235SFA MCU controls on-chip peripherals with a bootloader capability. The library performs peripheral initialization and control functions, with a choice of polled or interrupt- driven peripheral support. The DriverLib APIs in ROM can be called by applications to reduce flash memory requirements and free the flash memory to be used for other purposes.

#### 5.8.1.3 Flash Memory

The CC3235SF device within the BDE-WF3235SFA modules comes with an on-chip flash memory of 1MB that allows application code to execute in place while freeing SRAM exclusively for read-write data. The flash memory is used for code and constant data sections and is directly attached to the ICODE/ DCODE bus of the Arm Cortex-M4 core. A 128-bit-wide instruction prefetch buffer allows maintenance of maximum performance for linear code or loops that fit inside the buffer.

The flash memory is organized as 2-KB sectors that can be independently erased. Reads and writes can be performed at word (32-bit) level.

#### 5.8.1.4 Memory Map

Table 5-4 describes the various MCU peripherals and how they are mapped to the processor memory. For more information on peripherals, see the API document.

**Table 5-4. Memory Map**

| START ADDRESS | END ADDRESS | DESCRIPTION | COMMENT |
|---|---|---|---|
| 0x0000 0000 | 0x0007 FFFF | On-chip ROM (bootloader + DriverLib) | |
| 0x0100 0000 | 0x010F FFFF | On-chip flash (for user application code) | SF devices only |
| 0x2000 0000 | 0x2003 FFFF | Bit-banded on-chip SRAM | |
| 0x2200 0000 | 0x23FF FFFF | Bit-band alias of 0x2000 0000 to 0x200F FFFF | |
| 0x4000 0000 | 0x4000 0FFF | Watchdog timer A0 | |
| 0x4000 4000 | 0x4000 4FFF | GPIO port A0 | |
| 0x4000 5000 | 0x4000 5FFF | GPIO port A1 | |
| 0x4000 6000 | 0x4000 6FFF | GPIO port A2 | |
| 0x4000 7000 | 0x4000 7FFF | GPIO port A3 | |
| 0x4000 C000 | 0x4000 CFFF | UART A0 | |
| 0x4000 D000 | 0x4000 DFFF | UART A1 | |
| 0x4002 0000 | 0x4000 07FF | $I^2C$ A0 (master) | |
| 0x4002 4000 | 0x4002 4FFF | GPIO group 4 | |
| 0x4002 0800 | 0x4002 0FFF | $I^2C$ A0 (slave) | |
| 0x4003 0000 | 0x4003 0FFF | General-purpose timer A0 | |
| 0x4003 1000 | 0x4003 1FFF | General-purpose timer A1 | |
| 0x4003 2000 | 0x4003 2FFF | General-purpose timer A2 | |
| 0x4003 3000 | 0x4003 3FFF | General-purpose timer A3 | |
| 0x400F7000 | 0x400F 7FFF | Configuration registers | |
| 0x400F E000 | 0x400F EFFF | System control | |
| 0x400F F000 | 0x400F FFFF | µDMA | |
| 0x4200 0000 | 0x43FF FFFF | Bit band alias of 0x4000 0000 to 0x400F FFFF | |
| 0x4401 0000 | 0x4401 0FFF | SDIO master | |
| 0x4401 8000 | 0x4401 8FFF | Camera Interface | |
| 0x4401 C000 | 0x4401 DFFF | McASP | |
| 0x4402 0000 | 0x4402 0FFF | SSPI | Used for external serial flash |
| 0x4402 1000 | 0x4402 1FFF | GSPI | Used by application processor |
| 0x4402 5000 | 0x4402 5FFF | MCU reset clock manager | |
| 0x4402 6000 | 0x4402 6FFF | MCU configuration space | |
| 0x4402 D000 | 0x4402 DFFF | Global power, reset, and clock manager (GPRCM) | |
| 0x4402 E000 | 0x4402 EFFF | MCU shared configuration | |
| 0x4402 F000 | 0x4402 FFFF | Hibernate configuration | |
| 0x4403 0000 | 0x4403 FFFF | Crypto range (includes apertures for all crypto-related blocks as follows) | |
| 0x4403 0000 | 0x4403 0FFF | DTHE registers and TCP checksum | |
| 0x4403 5000 | 0x4403 5FFF | MD5/SHA | |
| 0x4403 7000 | 0x4403 7FFF | AES | |
| 0x4403 9000 | 0x4403 9FFF | DES | |
| 0xE000 0000 | 0xE000 0FFF | Instrumentation trace Macrocell™ | |
| 0xE000 1000 | 0xE000 1FFF | Data watchpoint and trace (DWT) | |
| 0xE000 2000 | 0xE000 2FFF | Flash patch and breakpoint (FPB) | |
| 0xE000 E000 | 0xE000 EFFF | NVIC | |
| 0xE004 0000 | 0xE004 0FFF | Trace port interface unit (TPIU) | |
| 0xE004 1000 | 0xE004 1FFF | Reserved for embedded trace macrocell (ETM) | |
| 0xE004 2000 | 0xE00F FFFF | Reserved | |

## 5.9 Restoring Factory Default Configuration

The module has an internal recovery mechanism that rolls back the file system to its predefined factory image or restoring the factory default parameters of the device. The factory image is kept in a separate sector on the sFLASH in a secure manner and cannot be accessed from the host processor. The following restore modes are supported:

- None—no factory restore settings
- Enable restore of factory default parameters
- Enable restore of factory image and factory default parameters

The restore process is performed by calling software APIs, or by pulling or forcing SOP[2:0] = 011 pins and toggling the nRESET pin from low to high.

The process is fail-safe and resumes operation if a power failure occurs before the restore is finished. The restore process typically takes about 8 seconds, depending on the attributes of the serial flash vendor.

## 5.10 Boot Modes

The BDE-WF3235SFA MCU implements a sense-on-power (SoP) scheme to determine the device operation mode.

SoP values are sensed from the module pin during power up. This encoding determines the boot flow. Before the device is taken out of reset, the SoP values are copied to a register and used to determine the device operation mode while powering up. These values determine the boot flow as well as the default mapping for some of the pins (JTAG, SWD, UART0). Table 5-5 lists the pull configurations.

BDE-WF3235SFA contains internal pulldown resistors on the SOP[2:0] lines. The application can use SOP2 for other functions after chip has powered up. However, to avoid spurious SOP values from being sensed at power up, we strongly recommends using the SOP2 pin only for output signals. The SOP0 and SOP1 pins are multiplexed with the WLAN analog test pins and are not available for other functions.

**Table 5-5. BDE-WF3235SFA Functional Configurations**

| NAME | SOP[2] | SOP[1] | SOP[0] | SoP MODE | COMMENT |
|---|---|---|---|---|---|
| UARTLOAD | Pullup | Pulldown | Pulldown | LDfrUART | Factory, lab flash, and SRAM loads through the UART. The device waits indefinitely for the UART to load code. The SOP bits then must be toggled to configure the device in functional mode. Also puts JTAG in 4-wire mode. |
| FUNCTIONAL_2WJ | Pulldown | Pulldown | Pullup | Fn2WJ | Functional development mode. In this mode, 2-pin SWD is available to the developer. TMS and TCK are available for debugger connection. |

| | | | | | |
|---|---|---|---|---|---|
| FUNCTIONAL_4WJ | Pulldown | Pulldown | Pulldown | Fn4WJ | Functional development mode. In this mode, 4-pin JTAG is available to the developer. TDI, TMS, TCK, and TDO are available for debugger connection. The default configuration for BDE-WF3235SFA MCU. |

**Table 5-5. BDE-WF3235SFA Functional Configurations (continued)**

| NAME | SOP[2] | SOP[1] | SOP[0] | SoP MODE | COMMENT |
|---|---|---|---|---|---|
| UARTLOAD_FUNCTIONAL_4WJ | Pulldown | Pullup | Pulldown | LDfrUART_FnWJ | Supports flash and SRAM load through UART and functional mode. The MCU bootloader tries to detect a UART break on UART receive line. If the break signal is present, the device enters the UARTLOAD mode, otherwise, the device enters the functional mode. TDI, TMS, TCK, and TDO are available for debugger connection. |
| RET_FACTORY_IMAGE | Pulldown | Pullup | Pullup | RetFactDef | When module reset is toggled, the MCU bootloader kickstarts the procedure to restore factory default images. |

## 5.11 Hostless Mode

The BDE-WF3235SFA device incorporates a scripting ability that enables offloading of simple tasks from the host processor. Using simple and conditional scripts, repetitive tasks can be handled internally, which allows the host processor to remain in a low-power state. In some cases where the scripter is being used to send packets, it reduces code footprint and memory consumption. The *if-this-then-that* style conditioning can include anything from GPIO toggling to transmitting packets.

The conditional scripting abilities can be divided into conditions and actions. The conditions define when to trigger actions. Only one action can be defined per condition, but multiple instances of the same condition may be used, so in effect multiple actions can be defined for a single condition. In total, 16 condition and action pairs can be defined. The conditions can be simple, or complex using sub-conditions (using a combinatorial AND condition between them). The actions are divided into two types, those that can occur during runtime and those that can occur only during the initialization phase.

The following actions can only be performed when triggered by the pre-initialization condition:

- Set roles AP, station, P2P, and Tag modes
- Delete all stored profiles
- Set connection policy
- Hardware GPIO indication allows an I/O to be driven directly from the WLAN core hardware to indicate internal signaling

The following actions may be activated during runtime:

- Send transceiver packet
- Send UDP packet
- Send TCP packet
- Increment counter increments one of the user counters by 1
- Set counter allows setting a specific value to a counter
- Timer control
- Set GPIO allows GPIO output from the device using the internal networking core
- Enter Hibernate state

---

**Note**

Consider the following limitations:

- Timing cannot be ensured when using the network scripter because some variable latency will apply depending on the utilization of the networking core.
- The scripter is limited to 16 pairs of conditions and reactions.
- Both timers and counters are limited to 8 instances each. Timers are limited to a resolution of 1 second. Counters are 32 bits wide.
- Packet length is limited to the size of one packet and the number of possible packet tokens is limited to 8.

---

# 6. Applications, Implementation, and Layout

## 6.1 Typical Application

### 6.1.1 BLE/2.4 GHz Radio Coexistence

The BDE-WF3235SFA device is designed to support BLE/2.4 GHz radio coexistence. Because WLAN is inherently more tolerant to time-domain disturbances, the coexistence mechanism gives priority to the Bluetooth® low energy entity over the WLAN. Bluetooth® low energy operates in the 2.4 GHz band, therefore the coexistence mechanism does not affect the 5 GHz band. The BDE-WF3235SFA device can operate normally on the 5 GHz band, while the Bluetooth® low energy works on the 2.4 GHz band without mutual interference.

The following coexistence modes can be configured by the user:

- Off mode or intrinsic mode
  - No BLE/2.4 GHz radio coexistence, or no synchronization between WLAN and Bluetooth® low energy—in case Bluetooth® low energy exists in this mode, collisions can randomly occur.
- Time Division Multiplexing (TDM, Dual Antenna)
  - Dual-band Wi-Fi (see Figure 6-1)

    In this mode, the WLAN can operate on either a 2.4 or 5 GHz band and Bluetooth® low energy operates on the 2.4 GHz band.

Figure 6-1 shows the dual antenna implementation of a complete Bluetooth® low energy and WLAN coexistence network with the WLAN operating on either a 2.4- or a 5 GHz band. Note in this implementation a Coex switch is not required and only a single GPIO from the BLE device to the BDE-WF3235SFA device is needed.

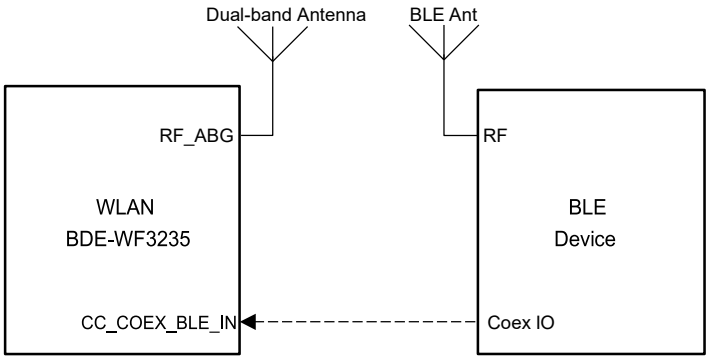


**Figure 6-1. Dual-Antenna Coexistence Mode Block Diagram**

### 6.1.2 Typical Application Schematic

Figure 6-2 shows the typical application schematic using the BDE-WF3235SFA module.

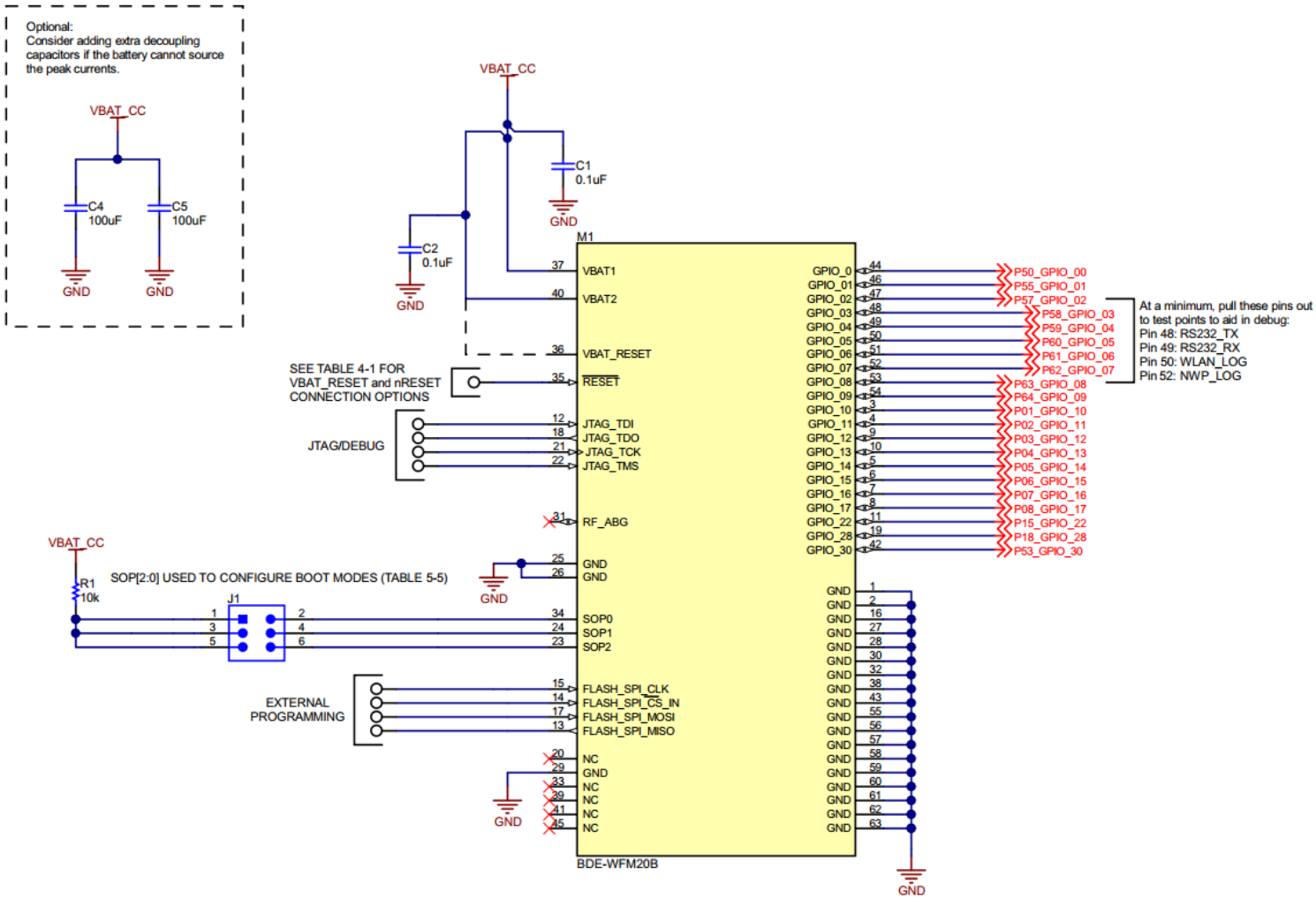


**Figure 6-2. BDE-WF3235SFA Typical Application Schematic**

Table 6-1 provides the bill of materials for a typical application using the BDE-WF3235SFA module in Figure 6-2.

**Table 6-1. Bill of Materials**

| QTY | PART REFERENCE | VALUE | MANUFACTURER | PART NUMBER | DESCRIPTION |
|---|---|---|---|---|---|
| 2 | C1, C2 | 0.1 µF | Murata | GRM155R61A104KA01D | Capacitor, ceramic, 0.1 µF, 10 V, ±10%, X5R, 0402 |
| 2 | C4, C5 | 100 µF | Murata | LMK325ABJ107MMHT | Capacitor, ceramic, 100 µF, 10 V, ±20%, X5R, AEC-Q200 Grade 3, 1210 |
| 1 | R1 | 10 k | Vishay-Dale | CRCW040210K0JNED | RES, 10k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 |
| 1 | M1 | BDE-WF3235SFA | BDE | BDE-WF3235SFA | Wi-Fi® and Internet-of-Things Module Solution, a Single-Chip Wireless Dual-Band MCU |

## 6.2 Device Connection and Layout Fundamentals

### 6.2.1 Power Supply Decoupling and Bulk Capacitors

Depending upon routing resistors and battery type, we recommend adding two 100-µF ceramic capacitors to help provide the peak current drawn by the BDE-WF3235SFA module.

**Note**

The module enters a brown-out condition whenever the input voltage dips below VBROWN (see Figure 4-1 and Figure 4-2). This condition must be considered during design of the power supply routing specifically if operating from a battery. For more details on brown-out consideration, see Section 4.5.

### 6.2.2 Reset

The module features an internal RC circuit to reset the device during power ON. The nRESET pin must be held below 0.6 V for at least 5 ms for the device to successfully reset.

### 6.2.3 Unused Pins

All unused pins can be left unconnected without the concern of having leakage current.

## 6.3 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the BDE-WF3235SFA. We recommend customers follow the guidelines described in this section to achieve similar performance to that obtained with the our reference design.

Ensure that the following general layout recommendations are followed:

- Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
- Do not run signal traces underneath the module on a layer where the module is mounted.

Use the following guidelines to lay out the BDE-WF3235SFA module with a PCB Trace Antenna, as shown in
Figure 6-3.

- The module must have a 6.2mm clearance on all layers (no copper) to the left and right of the module placement.
- There must be at least one ground-reference plane under the module on the main PCB.

**Figure 6-3. BDE-WF3235SFA Layout Guidelines**

# 7. Mechanical Specifications

## 7.1 Dimensions

The module dimensions are presented in the following figure:
Note: All dimensions are in mm

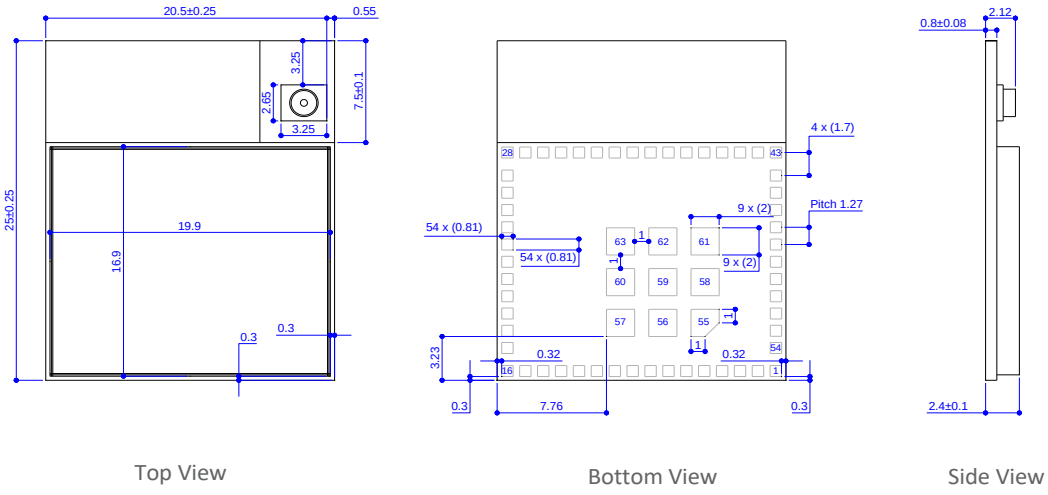


**Figure 7-1: Mechanical Drawing**

## 7.2 PCB Footprint

The footprint for the PCB is presented in the following figure:

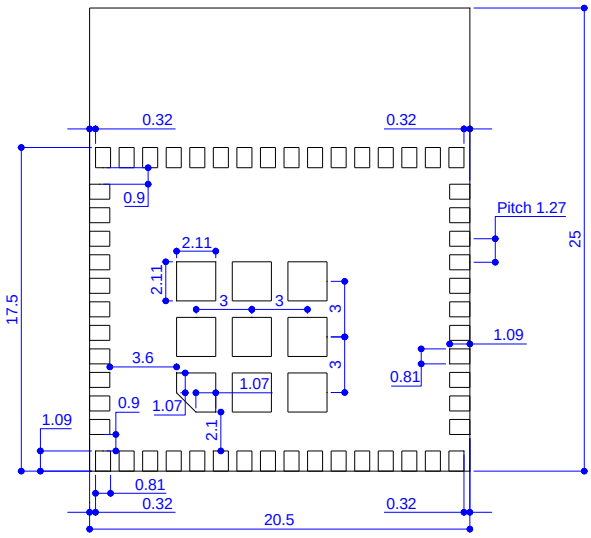


**Figure 7-2: Module Footprint Top View**

# 8. Ordering Information

**Table 10-1: Ordering Information**

| Part Number | Size (mm) | Shipping Form | MOQ |
|---|---|---|---|
| BDE-WF3235SFA | 20.5 x 25 x 2.4 | Tape & Reel | 1000 |

# 9. Revision History

| Revision | Date | Description |
|---|---|---|
| V1.0 | 27-July-2020 | Initial Released |
| V2.0 | 28-Dec-2021 | Changing the module name |
| V2.1 | 30-Aug-2023 | Picture, Size |

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